

Analog Modulo Integrator For Use In Open-Loop Sigma-Delta Modulators

Carsten Wulff, Øystein Knauserud, Trond Ytterdal

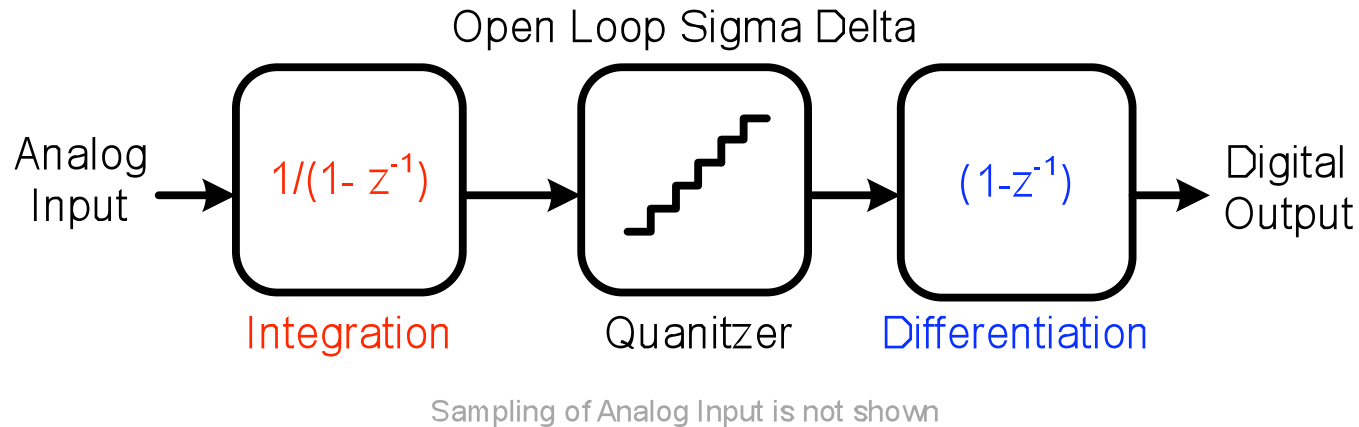
**Department of Electronics and Telecommunication
Norwegian University of Science and Technology**

Outline

- **Motivation for Open-Loop Sigma Delta Modulation (OLSDM)**
- **Analog Modulo Integrator**
- **Simulations of Analog Modulo Integrator**
- **Simulations of OLSDM**
- **Future Work**

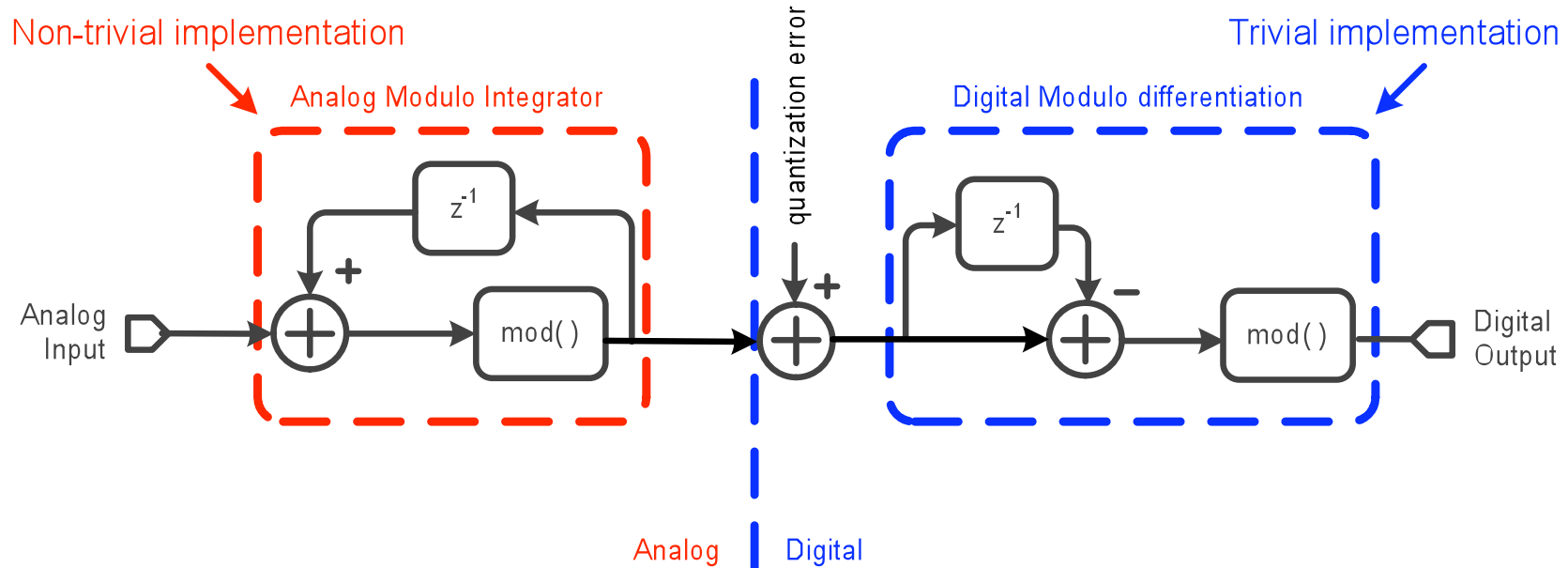
Motivation

- **What is Open-Loop Sigma Delta Modulation?**
 - It is Sigma Delta Modulation without global feedback, for low pass Sigma Delta it will be an integrator followed by a quantizer and a differentiator



- **Why do Open-Loop Sigma Delta?**
 - Removes feedback DAC, may potentially alleviate linearity problems in Sigma Delta modulators with multi bit quantizers

Analog-to-Digital OLSDM



- **Do an operation on analog side to limit signal swing (modulo integration), and do the inverse operation on the digital side (modulo differentiation)**
 - STF(Signal Transfer Function): digital output = analog input
 - NTF(Noise Transfer Function) : digital output = $(1-z^{-1})$ quantization error
- **Need to implement analog modulo integration:**
 - Frequency-to-digital Sigma-Delta Modulator [1]
 - Our approach: Make an analog modulo integrator

Conventional SC Integrator

- Charge C_1 during ϕ_1

$$Q_1(n) = C_1 \times V_i(n), \quad Q_2(n) = C_2 \times V_o(n)$$

- Transfer charge from C_1 to C_2 during ϕ_2

$$Q_2(n+1) = C_2 \times V_o(n+1) = Q_1(n) + Q_2(n) = C_1 \times V_i(n) + C_2 \times V_o(n)$$

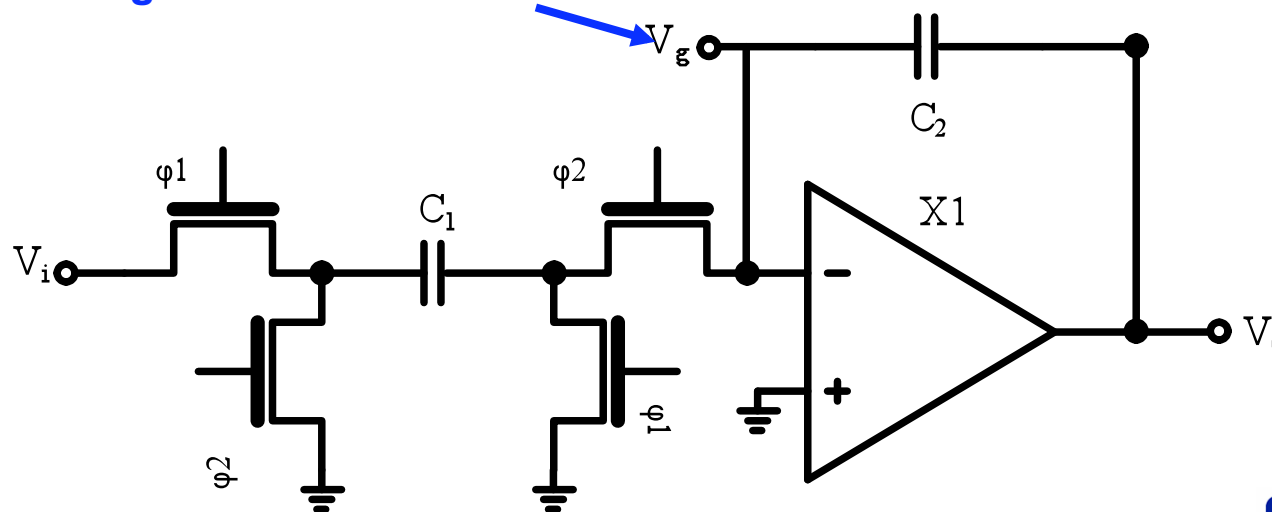
- Define : $-V_{ref} < V_o < V_{ref}$ and $C_1 = C_2$

$$V_o(n+1) = V_i(n) + V_o(n)$$

- If $V_i(n) = V_{ref} - \Delta$ and $V_o(n) = V_{ref} - \Delta$, where Δ is a small value, then charge transfer will be incomplete because opamp will saturate

- But the total charge: $Q_{total}(n+1) = Q_1(n) + Q_2(n) \approx C \times 2V_{ref}$ is preserved

Analog Modulo Circuit connected here



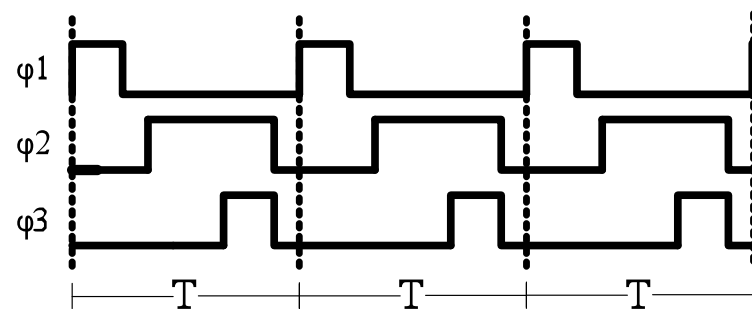
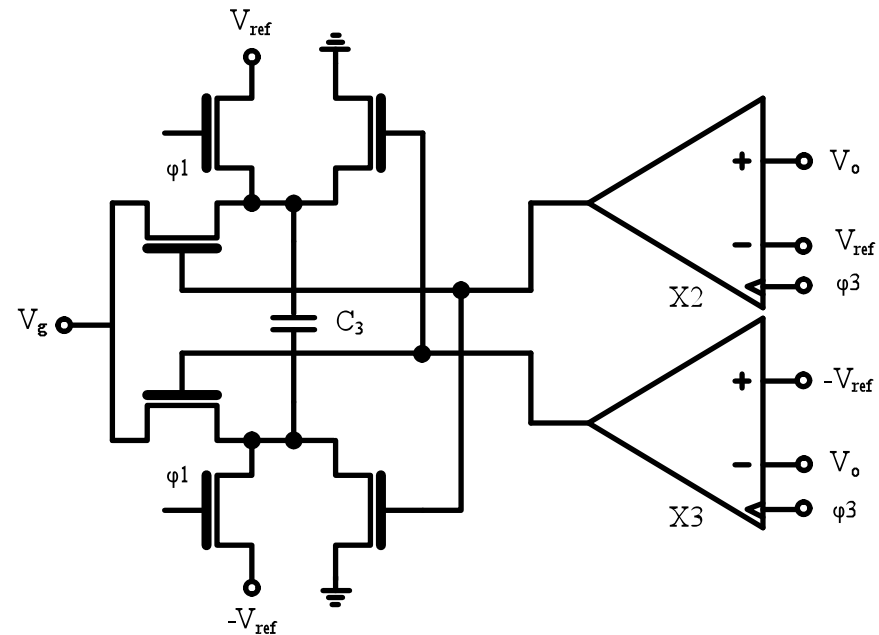
Analog Modulo SC Integrator (1)

- Phi1 and Phi2 stay the same
- In Phi3 the circuit detects whether V_o exceeds V_{ref} or $-V_{ref}$

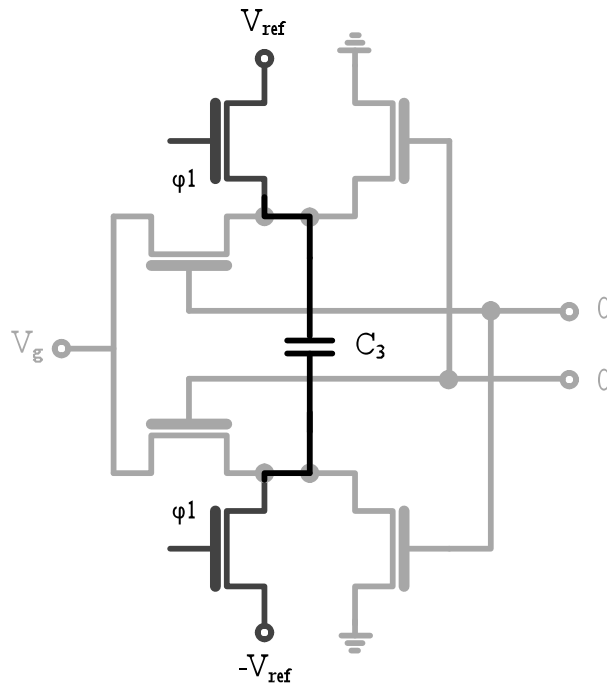
1. If $V_o \geq V_{ref}$ it subtracts $2xV_{ref}$
2. If $-V_{ref} < V_o < V_{ref}$ it does nothing
3. If $V_o \leq -V_{ref}$ it adds $2xV_{ref}$

Pseudo Code:

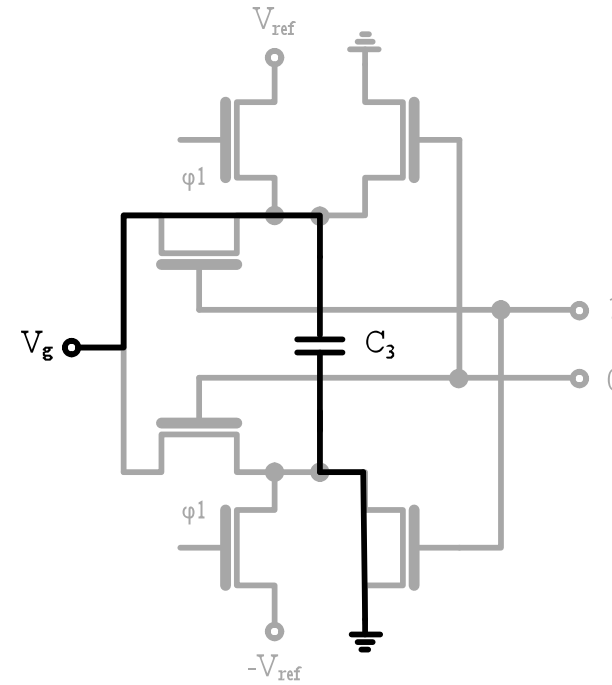
- Add the previous output to the current input
- If the new output exceeds the reference voltages
- Subtract/Add the range of the integrator, $V_r = 2xV_{ref}$
- Set the new output to the remainder



Analog Modulo SC Integrator (2)



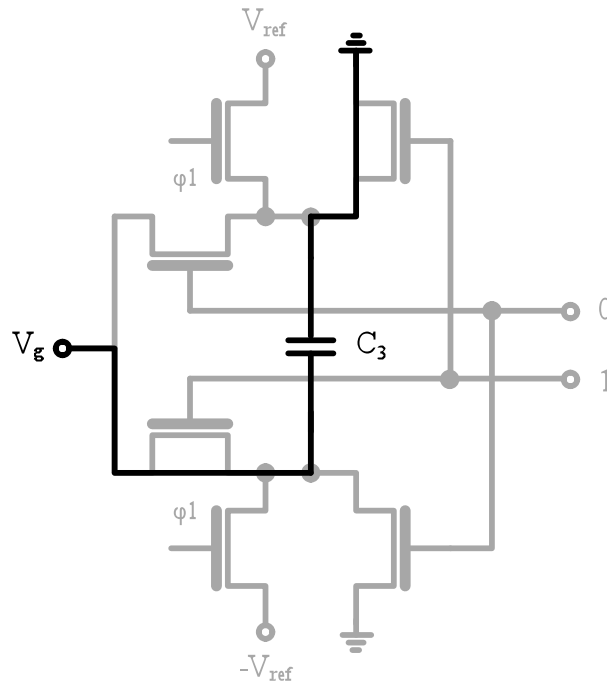
a) In $\phi 1$ the capacitor is charged.



b) In $\phi 3$, if $V_o \geq V_{ref}$ the charge transferred to V_g will be $Q_3 = C_3 V_r$

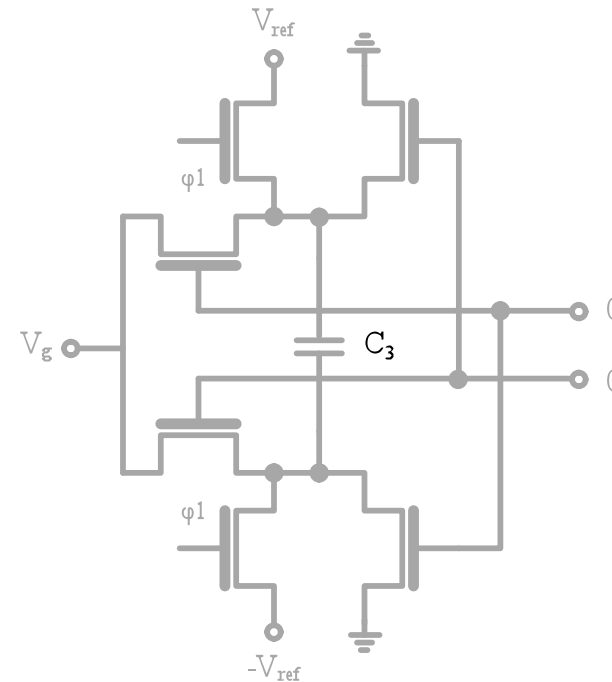
$$V_o(n+1) = V_i(n) + V_o(n) - V_r$$

Analog Modulo SC Integrator (3)



c) In ϕ_3 , if $V_o \leq -V_{ref}$ the charge transferred to V_g will be $Q_3 = -C_3 V_r$

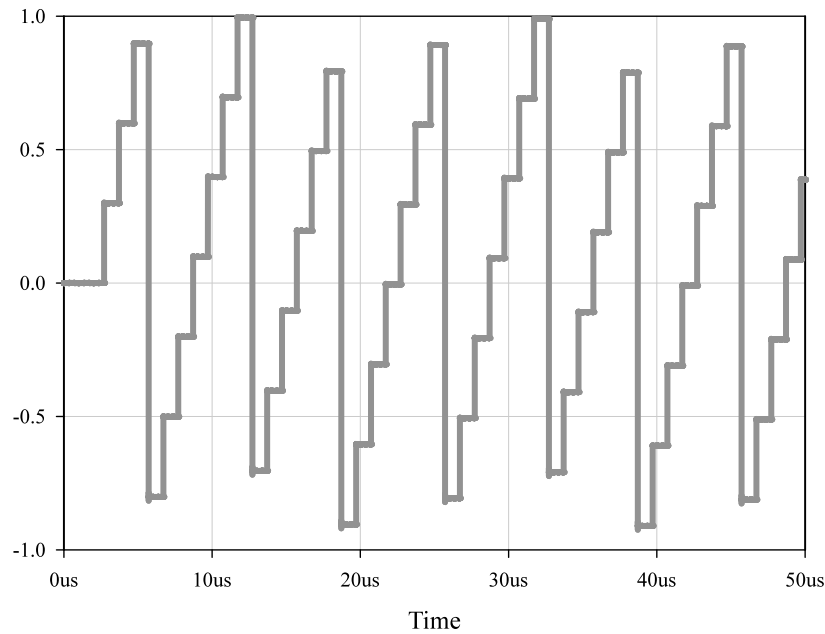
$$V_o(n+1) = V_i(n) + V_o(n) + V_r$$



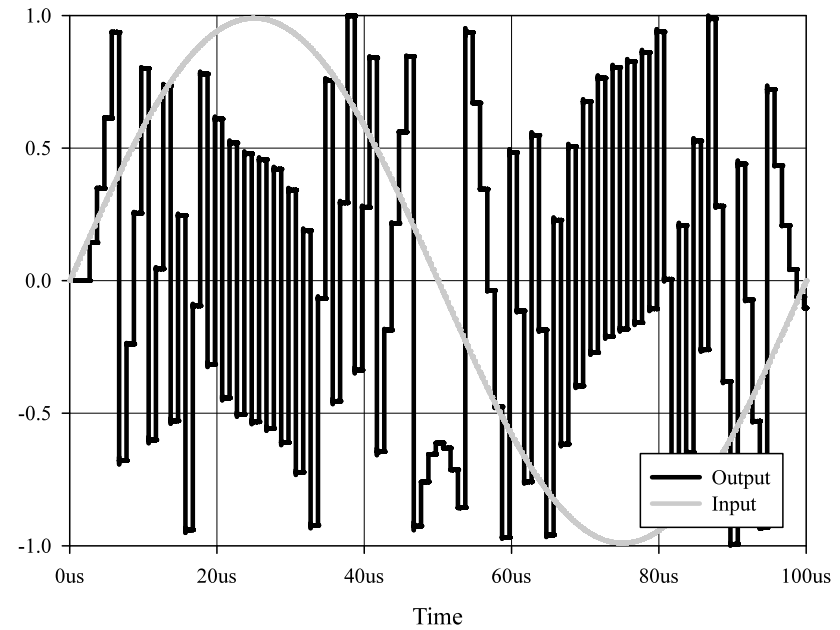
d) In ϕ_3 , if $-V_{ref} < V_o < V_{ref}$ no charge is transferred to C_3

$$V_o(n+1) = V_i(n) + V_o(n)$$

Simulations in AimSPICE[2]



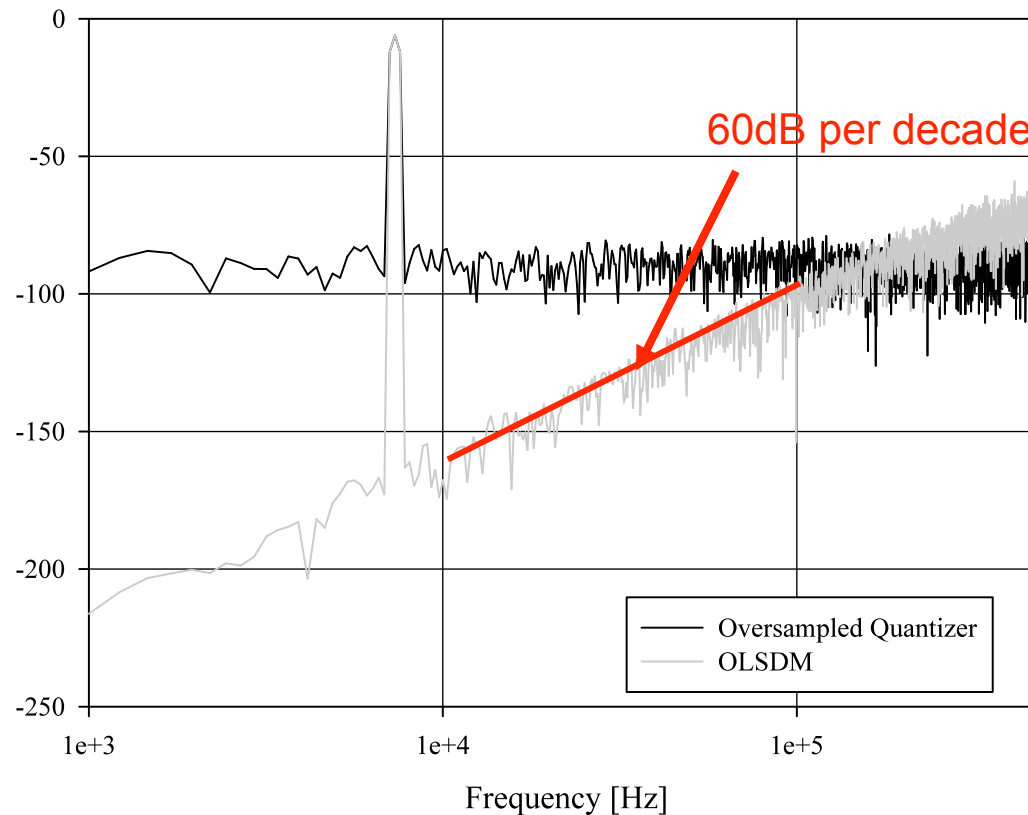
0.3V DC input



Sinusoidal input

The output never exceeds references $V_{ref}=1V$ and $-V_{ref}=-1V$

Simulations of OLSDM in SystemDotNet[3]



- **Third order OLSDM with 8 bit quantizer with OSR=8**
 - No noise shaping: ENOB = 9.5 bits
 - With noise shaping: ENOB = 15 bits

Future Work/Conclusion

- **Analog Modulo SC Integrator is (to our knowledge) a new circuit**
 - But as of yet, no show stoppers have been found
- **The Analog Modulo SC Integrator makes it possible to do OLSDM with conventional SC circuits**

References

1. M. Høvin, A. Olsen, T. S. Lande, and C. Toumazou, “Delta-sigma modulators using frequency -modulated intermediate values,” *IEEE J.Solid-State Circuits*, vol. 32, no. 1, pp. 13–22, 1997.
2. T. Ytterdal, “Aimspice,” <http://www.aimspice.com>
3. C. Wulff, “SystemDotNet,” <http://sourceforge.net/projects/systemdotnet>