Programmable Analog Integrated Circuit

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Abstract:

The prototype of a Programmable Analog Integrated Circuit (PAnIC) for use in remote laboratories is presented. The validity of using programmable analog integrated circuits to allow students to run remote experiments on different circuits is verified.

1. Introduction

When educating designers of integrated circuits it is essential to provide laboratories so an intuitive understanding of the underlying theory can be achieved. The test equipment for analog integrated circuits is often expensive, and to equip a laboratory to serve all students is impossible for most universities. Remotely operated laboratories provide a cost advantage in centralizing test equipment while providing students with decentralized concurrent access. Remotely operated laboratories have been explored in [1-8]. There exist remote laboratories that enable a student to make measurements on integrated circuits over the Internet. These laboratories often have a limitation on what types of integrated circuits or devices the student has access to. Some labs [6] have large switching matrixes to enable the student to select between different circuits that can be measured, others have a single integrated circuit with some tunable parameters [7,8]. As proposed in [9-11] we have explored a different route. Instead of using expensive switching matrixes, we have created a programmable analog integrated circuit (PAnIC) to provide a lab with circuit programmability.

2. Programmable Analog Integrated Circuits

The concept of a programmable analog integrated circuit is to have an integrated circuit with “standard” cells that can be wired into an analog circuit i.e. a filter or an amplifier. Figure 1 shows a very simple example of a programmable analog integrated circuit. By controlling a routing network that can connect the analog cells to each other, we can “build” analog circuits. Programmable analog integrated circuits have been reported since the early nineteen nineties. The earliest reference at IEEE is from 1991 [12]. Several manufactures have made programmable analog integrated circuits, among these are Motorola, IPM Inc, Lattice and Anadigm. Several designs of Field Programmable Analog Arrays (FPAA) have been reported [12-15], but these are often aimed at a commercial market as an analog counterpart to Field Programmable Gate Arrays (FPGA) for rapid prototyping of analog circuits. The marked for these FPAA have not gained the same momentum as FPGA, this because of the much greater challenges involved in creating an FPAA. One of the main challenges in creating FPAAs is the fact that analog circuits do not have a smallest common denominator. Digital circuits can (in theory) be created from NAND gates regardless of the complexity of the circuit. To circumvent this obstacle one can create expert cells [14, 15], where each analog cell has a set of tunable parameters i.e. a filter with tunable cut-off frequency. These expert cells are designed by analog designers and are guaranteed to operate within specification regardless of how they are connected to other cells. It is a modification of this approach that PAnIC has taken.

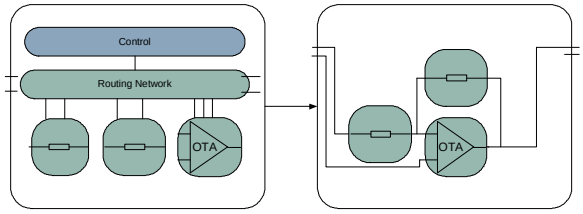

Figure 1 Programmable analog circuit concept

3. System overview

As mentioned above, the programmable analog integrated circuit provides a remote laboratory with a selection of different circuits that a student can perform experiments on. A system overview is shown in Figure 2. PAnIC is controlled by an AVR Microcontroller which is connected to a PC through an RS-232 serial interface. The PC runs a web service, which is program logic accessible over Internet via HTTP [16]. Web services based on Simple Object Access Protocol (SOAP) has seen a vast proliferation during the resent years. From all books on www.amazon.com directory [17] to experiments on electronic devices [6] are available over the Internet by the use of web services. The web service is consumed by a web server based on Microsoft .NET technology [18]. The system enables a student to run experiments on the analog cells in PAnIC over the Internet using nothing more than an Internet browser.

4. PAnIC Architecture

The PAnIC contains 6 analog cells; two digital to analog converters, one sample & hold amplifier, one comparator, one differential buffer and one bandgap voltage reference. Figure 3 shows a block diagram. The logic that enables programming of the PAnIC is divided

into a control block and analog module frameworks (AMF). The AMF is the core of the routing capabilities in PAnIC. They contain transmission gates, voltage buffers and digital logic for switching the transmission gates. These enable PAnIC to connect the analog cells to each other and to any of analog input/outputs. The main features of PAnIC are:

1. Four analog inputs and four analog outputs that can be connected to any of the analog cells.
2. Serial Peripheral Interface (SPI) and an 8 bit parallel IO for data communication.
3. Table of Content describing the analog cells.
4. Ability to discover all allowed connections between the analog cells through a feature called ReadBack.
5. Capable of driving 50 pF load on analog outputs.

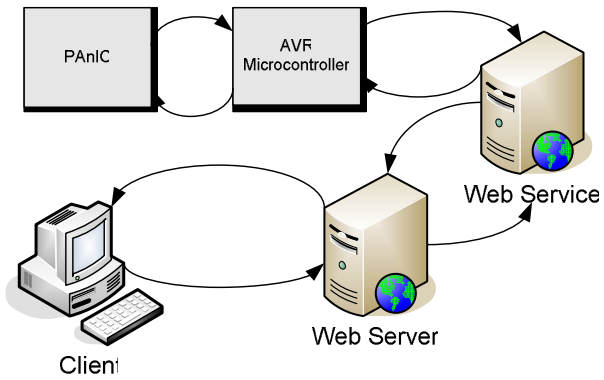

Figure 2 System Overview

The Table of Content and the ReadBack feature makes PAnIC a self-consistent circuit, information on how to control PAnIC and which connections it can make can be discovered. PAnIC was processed in a 0.6µm CMOS process, the chip measures 3.7mm x 4mm. A photograph of PAnIC can be seen in *Figure 4*. PAnIC covers the top portion of the chip and you can see the six analog modules; bandgap voltage reference (BGR), sample & hold (S&H), differential buffer (Buff), comparator (comp) and the two digital to analog converters (DAC1, DAC2). All analog cells, except the digital to analog converters, were designed by students in the Analog CMOS 2 course at NTNU in 2002.

5. Measured Results

The operation of the analog cells has been verified using the system described in section 3. The results for the digital to analog converter and successive approximation analog to digital converter are presented here. In Figure 5 the result of the digital to analog conversion is shown. One of the digital to analog converters was connected to the analog output and the digital input was stepped from 0-255 with a low reference voltage of 0V and a high reference voltage of 3V. As can be observed, the output is as expected for a digital to analog converter.

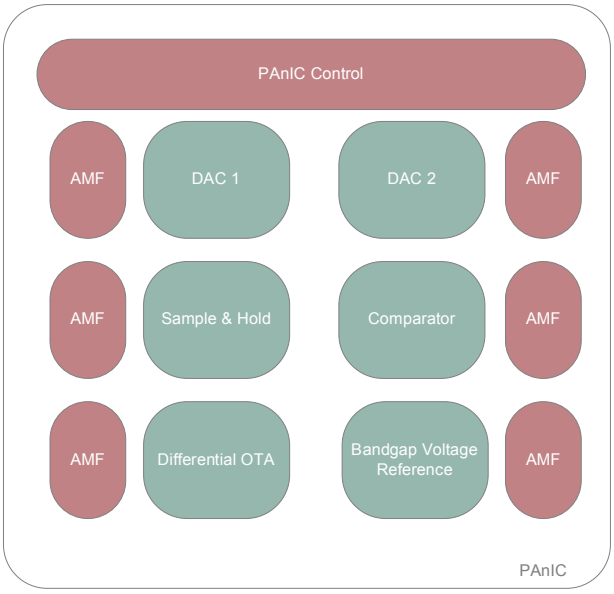

Figure 3 PAnIC block diagram

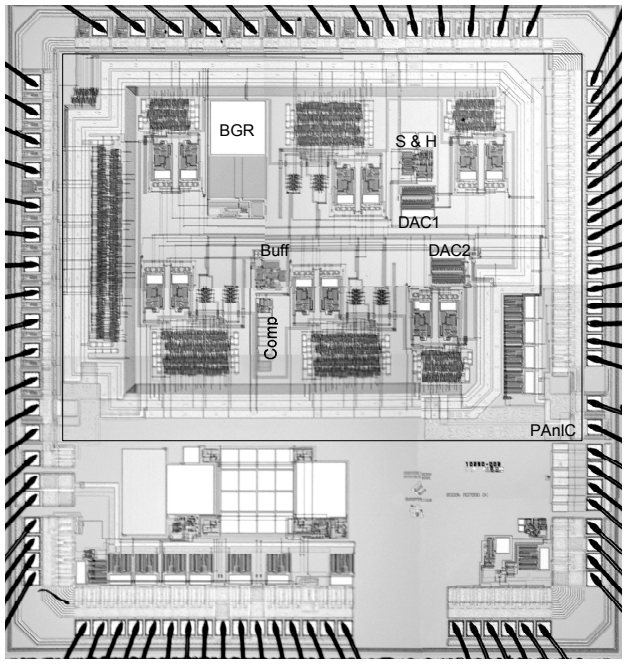

Figure 4 Photograph of the PAnIC chip

Figure 6 is the result of testing the successive approximation analog to digital converter. The comparator and one of the digital to analog converters were connected to each other and to the analog inputs/outputs as shown in Figure 7. It is important to keep in mind that the difference in test setup of the digital to analog converter and analog to digital converter consists simply of reprogramming PAnIC. The switch between these two setups is virtually instantaneous for a student using the web application. This allows a number of students to run different experiments at, what seems, the same time.

The microcontroller was used for control signals and ramping the input of the digital to analog converter. A frequency generator was connected to the input with a 10Hz signal. Although designed for 2 MSPS operation the ADC was not able to achieve this in our preliminary test. This was due too limited memory in the AVR microcontroller. The digital value had to be converted into ASCII and sent over RS-232 to the computer for each sample, which takes time. But since the speed of the ADC is not vital for demonstrating function for students, optimizing the speed has been left for future work.

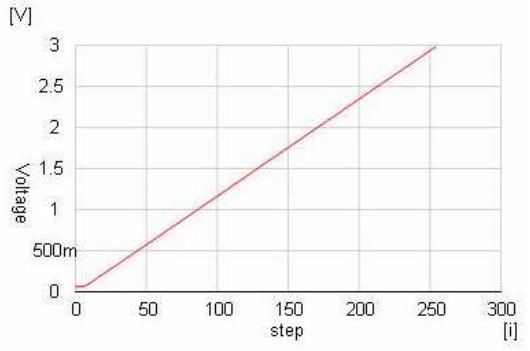

Figure 5 Measurement of the digital to analog converter

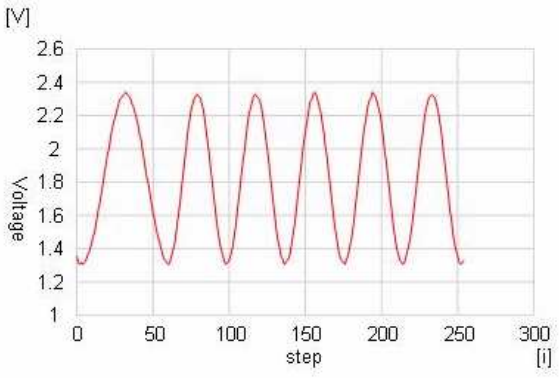

Figure 6 Measurement of the analog to digital converter

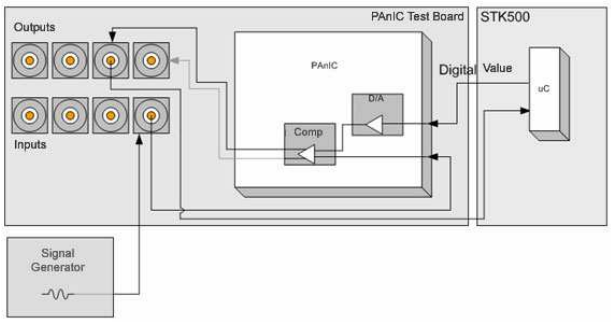

Figure 7 Connections during testing of ADC

6. Conclusion

The prototype of a Programmable Analog Integrated Circuit (PAnIC) for use in remote laboratories has been presented. The validity of using programmable analog integrated circuits to allow students to run experiments on different circuits has been verified.

7. Future Work

Current plans for PAnIC is to optimize the system from PAnIC chip to web application so it is suitable for being used as supplement to courses at the Department of Electronics and Telecommunication. One of the first experiments planned is to run Differential Nonlinearity and Integral Nonlinearity measurements on the digital to analog converters and the analog to digital converter. Thus enabling students to get an intuitive understanding of these two parameters, which are important in data converter design.

8. References

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