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Efficient ADCs for nano-scale CMOS Technology

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Faculty of Information Technology, Mathematics and Electrical Engineering
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Abstract

The topic of this thesis is efficiency of analog-to-digital converters (ADC) in nano-scale CMOS technology. With downscaling of CMOS technology it is harder to design ADCs. The power supply is reduced due to reliability concerns and the output resistance of transistors is reduced because of shorter channel lengths. Such challenges makes it harder to design ADCs with conventional circuit techniques and ADC architectures.

We investigate two separate paths towards higher efficiency in nano-scale CMOS technologies: circuit implementation, and ADC architectures.

The research into ADC architectures assumes that circuit implementation challenges will be solved. It looks at how a sigma-delta modulator can be used as a front-end to pipelined ADCs. A new class of sigma-delta modulators, the switched-capacitor (SC) open-loop sigma-delta modulator (OLSDM) is introduced. We introduce the SC modulo integrator and the SC modulo resonator that facilitates implementation of sigma-delta modulators that do not have feedback of the quantized signal. Thus, high-latency converters such as pipelined ADCs can be used as quantizers. Limitations of OLSDM, like operational amplifier (opamp) DC gain, quantizer linearity, and input signal amplitude are discussed in detail. Behavioral simulations of OLSDMs confirm the theory.

The research into circuit implementations investigate how the opamp can be removed from SC circuits. Two techniques are investigated: open-loop residue amplification and comparator-based switched-capacitor circuits (CBSC).

We present the design of a 7-bit 200MS/s 2mW pipelined ADC based on switched open-loop residue amplifiers. By turning off the open-loop

amplifiers when they are not needed the power dissipation is reduced by 23%.

Comparator-based switched-capacitor circuits (CBSC) are an alternative to opamp based SC circuits. By replacing the opamp with a comparator and current sources the same charge transfer is achieved.

We discuss design equations for CBSC, and how one can model CBSC in MATLAB and SPICE.

We present an 8-bit 60MS/s 8.5mW pipelined ADC with 7.05-bit effective number of bits (ENOB). At the time of writing it was the first silicon proven differential CBSC pipelined ADC.

Preface

This thesis was submitted to the Norwegian University of Science and Technology (NTNU) in partial fulfilment of the requirements for the degree of philosophiae doctor (PhD). The work presented herein was conducted at the Department Electronics and Telecommunication, NTNU, under the supervision of Professor Trond Ytterdal, with Professor Trond Sæther as co-advisor. Financial support from the Norwegian Research Council through the project Smart Microsystems for Diagnostic Imaging in Medicine (project number 159559/130) and the project ASICs for Microsystems (project number 133952/420) is gratefully acknowledged.

Research Path

This is a document that has been four years in the making. I began by my work in January 2004. The intent was to investigate calibration algorithms for micro-systems, with focus on genetic algorithms. But I strayed from this path and found analog-to-digital converters. The project Smart Microsystems for Diagnostic Imaging in Medicine (SMIDA) needed a low resolution high speed ADC, and I was asked to build it. This led to some initial work on dynamic comparators, opamps in 90nm CMOS and bootstrapped switches.

Wislands doctoral thesis (2003) on *Non-feedback Delta-Sigma modulators for digital-to-analog conversion* peaked my interest. We[1] wanted to see if we could apply the open-loop sigma-delta technique to analog-to-digital

[1] Trond Ytterdal and I

converters. We believed they could be used as front-ends to pipelined ADCs. In that respect, we developed techniques for switched-capacitor circuits.

At ISSCC 2006 the first comparator-based switched-capacitor circuit was published, and we immediately jumped on it. From the summer of 2006 to the summer of 2007 my time was dedicated to tape-out the first differential comparator-based switched-capacitor ADC. That year I was fortunate to spend my time at the University of Toronto as a visiting researcher. The time in Toronto inspired much of my work, like the open-loop residue amplifiers for pipelined ADC, and the continuous time bootstrapped switches.

My chip came back in January 2008, and most of the spring was spent on making the chip work. On the first day I got 4.2-bit ENOB, and it took me four months to get to 7.05-bit.

As these four and a half years draw to a close, I find that I am satisfied. In a sense I have come full circle with the genetic algorithm used to calibrate my ADC.

Acknowledgements

- To my wife, Anita, without her this thesis would not have seen the light of day. She was willing to move half way around the world with me, for which I am forever grateful.
- To my son, Villem, born during my years as a PhD student you have shown me that it's possible to get up at 05:30 A.M and still survive the day. This has been immensely helpful. Your smiles and hugs brighten my mood after a long day at work.
- To my late mother, my dad, my sisters and my extended family for your love and support.
- To my supervisor, Trond Ytterdal, he has always been available for questions and his guidance is valued. He has provided the resources necessary to do this work.
- To my co-advisor, Trond Sæther, for his support and convincing me that analog integrated circuits was the way to go.

- To my colleagues at Department of Electronics and Telecommunication, Circuits and Systems Group for lunch discussions, coffee sessions and support.

- To my fellow PhD students for many fun discussions: Øystein Gjermundnes, Ashgar Havashki, Are Hellandsvik, Tajeshwar Singh, Ivar Løkken, Anders Vinje, Saeeid Tahmasbi Oskuii, Linga Reddy Chenkeramaddi and Bertil Nistad.

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- A special thanks to Professors Ken Martin and David Johns for many useful questions and suggestions.

Comments on style

In a break from conventional page numbering this thesis start with page number 1 on the title page. In this digital age it is likely that this thesis will be read on a computer. As the title page is page one, the page numbers of the thesis will match the page numbers of the electronic document. I believe this will make the thesis easier to navigate.

Contents

List of Figures

List of Tables

List of abbreviations

ADC	Analog-to-digital converter
ADSL	Asymmetric digital subscriber line
ASIC	Application specific integrated circuit
CBSC	Comparator-based switched-capacitor
CMOS	Complementary metal oxide semiconductor
DAC	Digital-to-analog converter
DC	Direct current
DITS	Drain-induced threshold shift
DIBL	Drain-induced barrier lowering
DNL	Differential non-linearity
DRAM	Dynamic random access memory
ENOB	Effective number of bits
ERBW	Effective resolution bandwidth
FFT	Fast Fourier transform
FOM	Figure of merit
IC	Integrated Circuit
IEEE	Institute of Electrical and Electronics Engineers
INL	Integral non-linearity
IO	Input - Output
ISSN	International Standard Serial Number
ITRS	International Technology Road-map for Semiconductors
JSSC	Journal of solid state circuits
GPRS	General Packet Radio Service
LDI	Lossless discrete integrator
LSB	Least significant bit

LC-SDM	Low-pass Conventional Sigma-Delta Modulator
L-SDM	Low-pass Sigma-Delta Modulator
MASH	Multi-stAge noise SHaping
MDAC	Multiplying digital-to-analog converter
MOSFET	Metal oxide semiconductor field effect transistor
MSB	Most significant bit
NMOS	n-channel MOSFET
NTF	Noise transfer function
NTNU	Norwegian university of science and technology
NUD	Number of unit devices in parallel
OLSDM	Open-loop sigma-delta modulator or open-loop sigma-delta modulation
opamp	Operational amplifier
OSR	Oversampling ratio
PMOS	p-channel MOSFET
PSD	Power spectral density
RMS	Root mean square
SADC	Sub analog-to-digital converter
SAR	Successive approximation register
SC	Switched-capacitor
SDM	Sigma-delta modulation
SFDR	Spurious free dynamic range
SMIDA	Smart Microsystems for Diagnostic Imaging in Medicine
SNDR	Signal to noise and distortion ratio
SNR	Signal to noise ratio
SoC	System-on-Chip
SPICE	Simulation Program With Integrated Circuit Emphasis

List of appended papers

1. Analog Modulo Integrator For Use In Open-Loop Sigma-Delta Modulators

Carsten Wulff, Øystein Knauserud, Trond Ytterdal

In proceedings of the 24th NORCHIP Conference, 2006.

Nov. 2006 Pages 125 - 128

Digital Object Identifier 10.1109/NORCHP.2006.329259

2. Switched capacitor analog modulo integrator for application in open loop sigma-delta modulators

Carsten Wulff, Øystein Knauserud, Trond Ytterdal

Analog Integrated Circuits and Signal Processing

Springer Netherlands, ISSN 0925-1030

Volume 54, Number 2, Pages 121-131 February 2008

DOI 10.1007/s10470-007-9084-2

3. Resonators in open-loop sigma-delta modulators

Carsten Wulff and Trond Ytterdal

Submitted to IEEE Transactions on Circuits and Systems I: Regular Papers

4. 0.8V 1GHz Dynamic Comparator in Digital 90nm CMOS Technology

Carsten Wulff and Trond Ytterdal
In proceedings of the 23rd NORCHIP Conference, 2005.
21-22 Nov. 2005 Pages 237 - 240
Digital Object Identifier: 10.1109/NORCHP.2005.1597033

5. Design of a 7-bit 200MS/s, 2mW Pipelined ADC With Switched Open-Loop Amplifiers In a 65nm CMOS Technology

Carsten Wulff and Trond Ytterdal
In proceedings of the 25th NORCHIP Conference, 2007.
Digital Object Identifier 10.1109/NORCHP.2007.4481042

6. Design and Behavioral Simulation of Comparator-Based Switched Capacitor Circuits

Carsten Wulff and Trond Ytterdal
Accepted at NORCHIP 2008

7. An 8-bit 60-MS/s 8.5mW Differential Comparator-Based Switched-Capacitor Pipelined ADC in 90nm CMOS Technology

Carsten Wulff and Trond Ytterdal
Submitted to IEEE Journal of Solid State Circuits

The following papers have also been published. Because they fall outside the theme of this thesis they are not included in the thesis.

A Next Generation Lab - A Solution for remote characterization of analog integrated circuits

Carsten Wulff, Trond Ytterdal, Thomas Aas Saethre, Arne Skjevlan, Tor A. Fjeldly and Michael S. Shur

Fourth IEEE International Caracas Conference on Devices, Circuits and Systems, Aruba, April 17-19, 2002.

B Programmable Analog Integrated Circuit for use in remotely operated laboratories

Carsten Wulff and Trond Ytterdal
International Conference on Engineering Education, ICEE-2002
August 18-21, 2002, Manchester, U.K.

C Programmable Analog Integrated Circuit

Carsten Wulff, Roger Erstad and Trond Ytterdal
In Proceedings of the 22nd NORCHIP Conference, 2004.
Nov. 2002, Pages 99 - 102

D High Speed, High Gain OTA in a Digital 90nm CMOS Technology

Øyvind Berntsen, Carsten Wulff, Trond Ytterdal
In proceedings of 23rd NORCHIP Conference, 2005.
21-22 Nov. 2005

E Bootstrapped Switch In Low-Voltage Digital 90nm CMOS Technology

Christian Lillebrekke, Carsten Wulff and Trond Ytterdal
In proceedings of 23rd NORCHIP Conference, 2005.
21-22 Nov. 2005

F New Approach for Continuous Time Sigma Delta Modulators

Francisco Colodro, Marta Laguna, Carsten Wulff, Trond Ytterdal and Antonio Torralba
In proceedings of 23rd NORCHIP Conference, 2005.
21-22 Nov. 2005

Chapter 1

Introduction

How can we make efficient analog-to-digital converters (ADCs) in nano-scale CMOS? Challenges like reduced headroom and reduced output resistance has made it hard to design efficient ADCs in the new nano-scale CMOS technologies. Why do we want more efficient ADCs? The simple answer is: longer battery life. The ADC is a key component in any signal chain that interface with the real world. The receive chain of GPRS networks, Wi-Fi networks, indeed any current mobile wireless communication technology has an ADC. Most of the processing today is done in the digital domain. The pure analog signal chains have been banished to obscurity. But the real world is analog, and information from the real world must be converted to digital before it can be digitally processed.

Consumers demand high speed mobile networking on the bus to work, at the local cafe, and in their homes. They want their portable devices to have infinite battery lives, and they should cost nothing. To reduce the cost and increase efficiency there has been a push for integration of features on a single chip (System-on-Chip). In SoCs with high integration most of the functions are digital, thus technologies that allow cheap integration of digital features are used. These are the nano-scale technologies (less than 100nm transistor gate length).

Reliability concerns of downscaled CMOS transistors has lead to a decrease in power supply. At high electrical fields the transistor gate oxide

breaks down. In downscaled transistors the thickness of the gate oxide is reduced, hence the maximum power supply must be reduced. Fig. 1.1 shows the historic power supply and future trends (from ITRS 2007 [1]). At the 250nm gate length the power supply is 2.5V, but in 90nm the power supply is reduced to 1.2V.

A challenge with reduced power supply is the reduced signal swing, in most cases the signal swing cannot be larger than the power supply. The accuracy of an ADC is proportional to sampling capacitance[1], and sampling capacitance is inversely proportional to the square of the signal swing. Hence, the capacitor size quadruples when we go from 250nm to 90nm CMOS technology for the same accuracy. An increased capacitor size result in higher area consumption and increased cost.

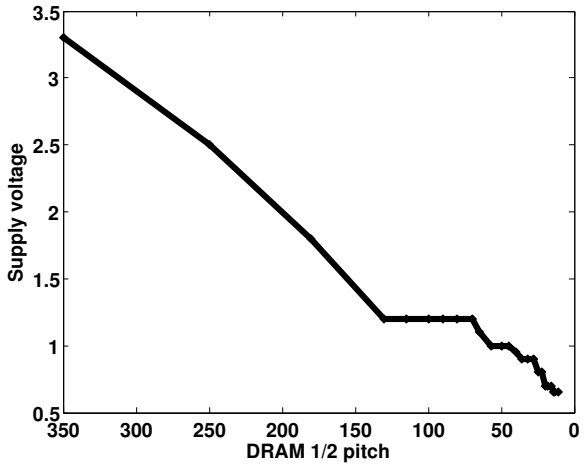

Fig. 1.1: Historic and future scaling of power supply (based on ITRS 2007 [1]). DRAM 1/2 pitch is smallest half-pitch of contacted metal lines in a DRAM cell.

Another challenge is the reduced output resistance of nano-scale CMOS transistors. As devices are scaled down the transistor channel lengths

[1]This is easily seen from the equation

$$S/R = \frac{Signal\ Power}{Noise\ Power} = \frac{A^2/2}{kT/C} = \frac{A^2C}{2kT} \tag{1.1}$$

shorten. At shorter channel lengths channel length modulation and drain induced barrier lowering [2] reduce the output resistance of the transistor. Longer channels can be used to increase the output resistance, but the effectiveness of using a longer channel is reduced by the pocket implants [3]. Pocket implants are used to reduce V_T roll-off and punch-through in nano-scale technologies. Due to the pocket implants the output resistance of a 1μm long transistor in a 90nm technology is lower than a 1μm long transistor in a 350nm technology.

For high accuracy circuits we need high gain in our transistors. The gain in a transistor is proportional to the output resistance of the transistor. The gain of the single transistor is called the intrinsic gain. It is defined as $A_i = g_m/g_{ds}$, where g_m is the transconductance and g_{ds} is the output conductance (inverse of output resistance). When the output resistance is reduced the intrinsic gain goes down, and in 65nm technology the intrinsic gain of a minimum device is 6[2] (15-dB). In 350nm technology a minimum device has a gain of 43[3] (32-dB). As a result, one must use multiple stages, cascoding, or gain boosting to achieve high gain amplifiers in 65nm technology. But techniques like cascoding (stacking transistors) is hard in 65nm technology due to the low supply voltage.

Downscaling of analog circuits is not all bad. The speed can be increased due to shorter channel lengths, and the parasitic capacitances are smaller. But these two advantages are overshadowed by the reduction in gain and power supply.

We believe that efficiency in nano-scale technology is best attacked from both ends: the circuit implementation, and the ADC architecture.

One approach to efficiency is to investigate the architectural level. If we assume that the circuit challenges can be solved, can we do anything about the ADC architectures? High accuracy (14-bit) high-speed ($>$ 10MS/s) ADCs are challenging to implement in nano-scale technologies because of the large sampling capacitors. With a 1V input signal swing the sampling capacitors will be 53pF for a 14-bit converter, which is a large capacitor.

[2] $L = 0.06$, $W = 10L$, $V_{DS} = V_{DD}/2$, $V_{EFF} = V_{DD}/8$, typical corner
[3] $L = 0.35$, $W = 10L$, $V_{DS} = V_{DD}/2$, $V_{EFF} = V_{DD}/8$, typical corner

To reduce the sampling capacitor we can use oversampling. In sigma-delta modulators oversampling is used in addition to quantization noise shaping to achieve high accuracy. We wanted to investigate a class of sigma-delta modulators called *Open-Loop Sigma-Delta Modulators* (OLSDM), and their use as a front-end to pipelined ADCs. The part of this thesis that focus on OLSDM is of a theoretical nature.

The other approach to increased efficiency is to investigate the circuit implementation. Switched-capacitor (SC) circuits are ubiquitous in ADCs. They are a tried and tested accurate method of implementing high speed ADCs. The sigma-delta modulators and pipelined ADCs predominate in the use of SC circuits. The traditional approach to SC circuits use opamps, which consume most of the power in an ADC. In nano-scale technology opamps have become increasingly hard to design due to the reduced headroom and decreased output resistance. Techniques that replace opamps have received interest from the research community. Part of this thesis investigate how one can replace opamps in pipelined ADCs, and through this improve efficiency. This part of the thesis is a combination of theoretical work and measurements on a nano-scale CMOS ADC.

1.1 Main contributions

The main contributions of this thesis are:

- We introduce the switched-capacitor modulo integrator. It facilitates implementation of switched-capacitor open-loop sigma-delta modulators.

- We introduce the switched-capacitor open-loop sigma-delta modulator. A versatile type of sigma-delta modulator suited as front-end to pipelined ADCs

- We introduce the modulo resonator. It enables implementation of high resolution open-loop sigma-delta modulators with low oversampling ratio.

- We prove that open-loop sigma-delta modulation is equivalent to sigma-delta modulation if

$$|x_n| < R\left(\frac{1}{2} - \frac{2^{N-1}}{2^B}\right) \tag{1.2}$$

  where x_n is the input signal at time n, R is the full scale range, N is the order of the modulator and B is the number of bits in the quantizer.

- We introduce the switched open-loop residue amplifiers. Using these the power dissipation is reduced by 23% for a 7-bit pipelined ADC.

- We introduce the first fully differential silicon proven comparator-based switched-capacitor pipelined ADC. Differential implementation allow higher signal swing, which is essential in nano-scale technologies.

Other significant contributions are:

- We present a comprehensive figure of merit survey of ADCs in Journal of Solid State Circuits (1975-2008) and International Solid State Circuits conference (2000-2008).

- We present the limits of figure of merit for ADCs

- We present design equations for comparator-based switched-capacitor circuits.

- We introduce a simple calibration scheme for comparator threshold calibration. This technique cancels the overshoot in comparator-based switched-capacitor pipelined ADCs

1.2 Thesis outline

This thesis is a collection of papers, hence the results are in the papers. The research presented in this thesis is on analog-to-digital converters, with focus on pipelined ADCs and sigma-delta modulators. If this subject is unfamiliar we suggest reading Chapters 9, 10, 11, 13 and 14 in [4].

This thesis is organized as follows: Chapter 2 discuss the fundamental limits of ADC figure of merit, and how parasitic capacitance make it hard to implement a low resolution converter with high efficiency.

In Chapter 3 the papers are introduced and we detail how the papers are related. The papers are presented in Chapter 4 to Chapter 10. Comments to papers, a conclusion and further work is presented in Chapter 11

Chapter 2

Limits of ADC figure of merit

Efficiency is one of the key measures of analog-to-digital converters. A more efficient ADC can translate into longer battery life of our hand-held devices. For ADCs the power dissipation (P), sampling frequency (f_s) and effective number of bits (B) are combined to give a single measure of the efficiency, the figure of merit (FOM). For the figures of merit discussed here a smaller value is better.

The historic figure of merit proposed by Walden [5] was (2.1)[1]

$$FOM = \frac{P}{2^B f_s} \tag{2.1}$$

This FOM, however, is incorrect if we assume the ADCs should be limited by thermal noise. A more correct figure of merit is

$$FOM = \frac{P}{2^{2B} f_s} \tag{2.2}$$

This figure of merit, the Thermal FOM, is based on the fact that in an ADC limited by thermal noise we must use 4 times the power if we add one bit of resolution, since the required sampling capacitance increases 4 times.

[1] It was actually presented as $FOM = 2^B f_s/P$, but the inverse is the most used.

A more in-depth argument is given in [6] on page 360.

If we have the ADC parameters (accuracy, power dissipation, speed) we can calculate the FOM from (2.2). But what is the limit of the FOM? How low FOM can we expect to get with future ADCs?

We will in this chapter derive expressions for the FOM limit and compare the limit to results of published ADCs. But first we have to derive the required sampling capacitance for a certain resolution.

2.1 Required sampling capacitance

We assume a switched-capacitor based ADC. The input signal is sampled across a sampling capacitor (C). And C is the only capacitor in the ADC. In such a system the thermal noise power can be represented as

$$\overline{V_{thermal}^2} = a_1 \times kT/C \tag{2.3}$$

where a_1 is a constant greater than one, k is Boltzmann's constant, T is the temperature in Kelvin and C is the sampling capacitance.

The thermal noise power should be less than the quantization noise power, but not too small, because a small thermal noise power will cost in terms of power dissipation. We assume that the quantization noise power is four times the thermal noise power.

$$\overline{V_{LSB}^2} = 4 \times \overline{V_{thermal}^2} \tag{2.4}$$

where $\overline{V_{LSB}^2}$ is the quantization noise power, which can be calculated as

$$\overline{V_{LSB}^2} = V_{LSB}^2/12 = V_{PP}^2/(2^{2B} \times 12) \tag{2.5}$$

where V_{LSB} is the voltage step of the least significant bit (LSB) and V_{PP} is the peak-to-peak input signal voltage.

If we combine (2.3), (2.4) and (2.5) we get

$$\frac{V_{PP}^2}{2^{2B} \times 12} = 4 \times a_1 \times kT/C \tag{2.6}$$

Solved for sampling capacitance (C) (2.6) becomes

$$C = a_1 \times \frac{48kT2^{2B}}{V_{PP}^2} \tag{2.7}$$

Using equation (2.7) we can calculate how large C must be for a certain resolution. For example for $V_{PP} = 1\,V, T = 300\,K$ we get $C_{[B=6]} = 0.8fF$, $C_{[B=12]} = 3.3pF$, and $C_{[B=14]} = 53pF$.

Assume the capacitor is used in a switched capacitor circuit, and that an amplifier is used to charge the capacitor to its final value. We will consider two methods for this capacitance to reach its final value: a constant ramp, and linear settling. Constant ramp is equivalent to what is used in comparator-based switched-capacitor circuits. Linear settling is equivalent to what is used in opamp based switch-capacitor circuits and open-loop residue amplifiers.

2.2 Constant ramp FOM limit

For a constant ramp the voltage across C is given by

$$V_o(t) = \frac{I}{C} \times t \tag{2.8}$$

where $t = 1/2f_s$, I is the current used to charge the capacitor, and f_s is the sampling frequency.

The maximum $V_o(t)$ is equal to V_{PP}, and will require the most time. Accordingly, we set $V_o(t) = V_{PP}$, insert for (2.7) in (2.8), and multiply each side with V_{DD}

$$V_{PP}V_{DD} = \frac{IV_{DD}V_{PP}^2}{96a_1kT2^{2B}f_s} \tag{2.9}$$

Solved for FOM (2.9) becomes

$$FOM_{ramp} = \frac{P}{2^{2B}f_s} = \frac{96a_1kT}{\frac{V_{PP}}{V_{DD}}} \tag{2.10}$$

This FOM does not depend on the number of bits (B) or the sampling

frequency (f_s).

2.3 Linear settling FOM limit

We assume the voltage across C must reach a final value within a certain accuracy, given by the LSB, and reach this accuracy within half the sampling period ($1/2f_s$).

Assume a transconductance amplifier (an ideal transistor with resistive load $R_o = 1/g_m$) is used to drive the capacitance C. The amplifier has the transfer function

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{1 + sC/g_m} \tag{2.11}$$

where V_o is the voltage across the capacitance, V_i is the input signal voltage, and g_m is the transconductance.

Assume the input is a unit step function $V_i(t) = V_{PP}u(t)$. The output will then be

$$V_o(t) = V_{PP} - V_{PP}e^{-g_m t/C}, t > 0 \tag{2.12}$$

Written in terms of the settling error ($\epsilon = V_{PP} - V_o(t)$) we get

$$\epsilon = V_{PP}e^{-g_m t/C} \tag{2.13}$$

The settling error (ϵ) should be smaller than one LSB, $\epsilon < V_{PP}/2^B$, but to simplify we set $\epsilon = LSB$. The transconductance in (2.13) can be written as $g_m = \eta_1 2I_D/V_{EFF}$ where η_1 is a technology dependent constant (it depends on high field effects and short channel effects, η_1 is larger than zero, but less than one. For a 90nm process it's around 0.5-0.6), I_D is the drain current and V_{EFF} is the effective gate overdrive. Inserted into (2.13) together with (2.7) results in

$$\frac{V_{PP}}{2^B} = V_{PP}\, e^{\left(-\frac{\eta_1 2 I_D \frac{V_{PP}^2}{V_{DD}^2} V_{DD}^2}{2 f_s \frac{V_{EFF}}{V_{DD}} V_{DD} a_1 48 k T 2^{2B}} \right)} \tag{2.14}$$

Solved for FOM we get

$$FOM = \frac{I_D V_{DD}}{2^{2B} f_s} = \frac{B \ln(2) \frac{V_{EFF}}{V_{DD}}}{\eta_1 \frac{V_{PP}^2}{V_{DD}^2}} a_1 48kT \tag{2.15}$$

According to this equation, it will be more difficult to get a good figure of merit with additional bits, but this ignores the influence of parasitic capacitances.

2.4 FOM limit including parasitic capacitance

Assume that an ADC has as many stages as bits (B), define M_0 as the number of circuit nodes per stage and C_0 as the parasitic capacitance per node. The total parasitic capacitance in the ADC will then be

$$C_p = C_0 M_0 B \tag{2.16}$$

The parasitic capacitance (2.16) will add to the load of our transconductance amplifier, accordingly the load will be

$$C = a_1 \times \frac{48kT 2^{2B}}{V_{PP}^2} + C_0 M_0 B \tag{2.17}$$

Inserted into (2.13)

$$\frac{V_{PP}}{2^B} = V_{PP}\, e^{\left(-\frac{\eta_1 2 I_D}{2 f_s \frac{V_{EFF}}{V_{DD}} V_{DD}} \frac{1}{\frac{a_1 48kT 2^{2B}}{V_{PP}^2} + C_0 M_0 B} \right)} \tag{2.18}$$

And with some manipulation

$$FOM = \frac{B \ln(2) \frac{V_{EFF}}{V_{DD}}}{\eta_1 \frac{V_{PP}^2}{V_{DD}^2}} \left(a_1 48kT + \frac{C_0 M_0 B V_{PP}^2}{2^{2B}} \right) \tag{2.19}$$

For $C_0 = 0$ (2.19) reduces to (2.15).

These three equations: (2.10), (2.15), and (2.19), are based on numerous assumptions, and it is interesting to see how well the equations predict published results for ADCs.

2.5 Comparison with published results

The FOM limits have been compared to selected ADCs published in Journal of Solid State Circuits (JSSC) in the years 1975-2008.[2] And selected ADCs published at the International Solid State Circuits Conference (ISSCC) in the years 2000-2008.

The comparison is shown in Fig. 2.1. We have used $V_{EFF}/V_{DD} = 1/8, V_{PP}/V_{DD} = 0.5, \eta_1 = 0.5, a_1 = 1, T = 300\ K$. Choosing the value for M_0 and C_0 is guesswork since they depend on ADC architecture and technology, but it is unlikely that $M_0 < 10$ and $C_0 < 1fF$. A more realistic model would arguably be $M_0 = 200$ and $C_0 = 10fF$.

None of the published ADCs go below the FOM limit given by (2.15) or (2.10), but for high number of bits ($>$ 14-bits) they begin to approach the limit. At high number of bits it is more straightforward to achieve a good FOM because the required sampling capacitor becomes large and the parasitic capacitances become less important. But for low to medium number of bits ($<$ 12-bits) the required sampling capacitance is so low ($<$ 4 pF) that the parasitic capacitances dominate.

At 7-bit the best ADC is more than 100 times worse than the FOM limit.

The parasitic FOM limit given by (2.19) match the shape of the data points. The realistic model ($M_0 = 200, C_0 = 10fF$) enclose most of the data points, and the likely limit ($M_0 = 10, C_0 = 1fF$) enclose all.

For ENOB larger than six bits constant ramp has an advantage over linear settling.

[2] The data for this study can be downloaded from `http://www.wulff.no/carsten` *Electronics, ADC FOM*

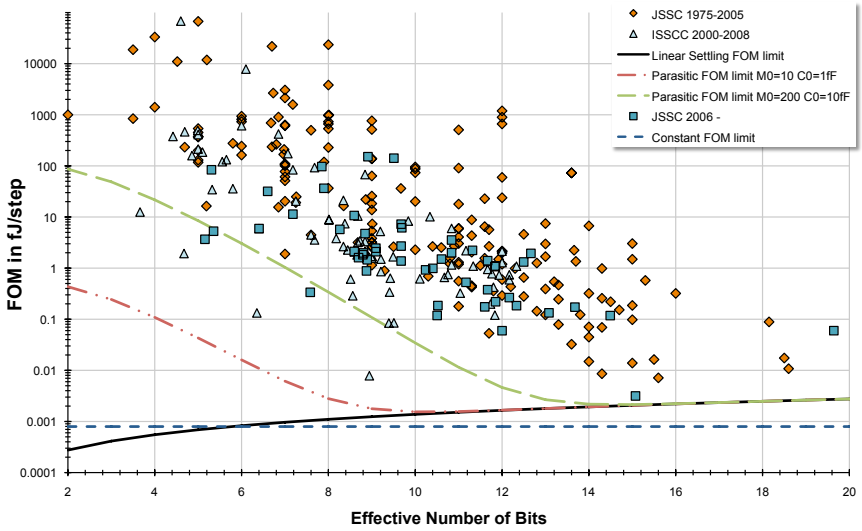

Fig. 2.1: FOM versus bits for selected ADCs published in JSSC in the years 1975-2008 and ADCs published at ISSCC 2000-2008 compared to: the FOM limit for constant ramp, FOM limit for linear settling, and the parasitic FOM model

Chapter 3

Research Overview

The research in this thesis is presented in seven papers. Fig. 3.1 shows how the papers are related. Papers 1, 2, 4, 5 and 6 are published works, while 3 and 7 are submitted for publication. The format of all papers have been modified to suit this thesis. The references for each paper has been included into the complete reference list at the end of the thesis. The content of papers 1, 2, 4, 5 and 6 have not been modified in any way from the published version.

The topic of the research is efficient ADCs in nano-scale CMOS technology. We focus on two separate paths:

1. Assume switched-capacitor implementation challenges will be solved and investigate ADCs with sigma-delta modulator front-end and pipelined back-end.

2. Investigate efficient circuit solutions for pipelined ADCs

The first path include papers 1, 2 and 3 while the second path include papers 4, 5, 6 and 7. We will describe the two paths separately.

3.1 Open-loop sigma-delta modulators (OLSDM)

The open-loop sigma-delta modulators in this thesis brings the OLSDM architecture to switched-capacitor architectures. Our motivation for creating

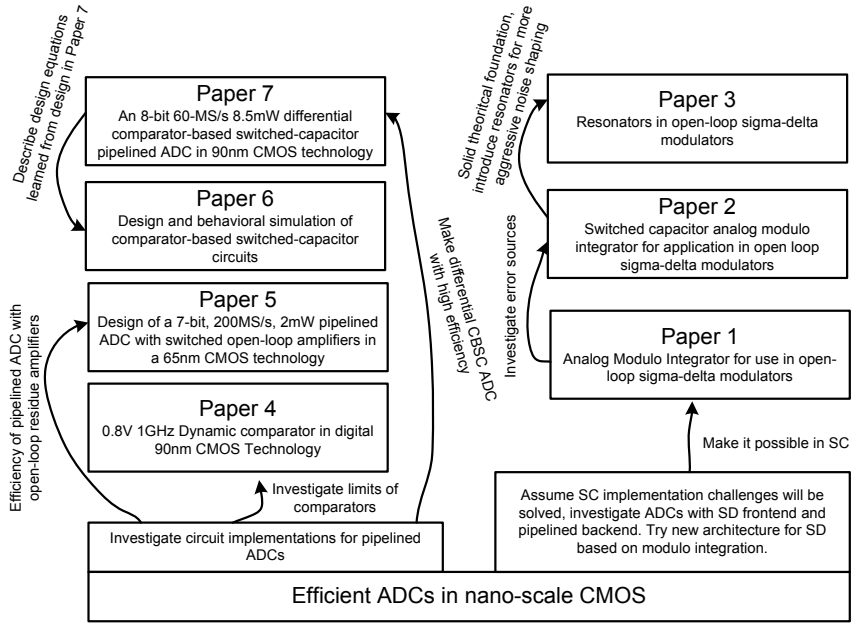

Fig. 3.1: How papers relate to each other and the central theme

an OLSDM is the use in hybrid converters. The idea is to use an OLSDM front-end and pipelined ADC back-end. Such hybrid converters can achieve good performance [7]. Previous OLSDM architectures have been digital-to-analog modulators [8], or frequency sigma-delta modulators [9].

Fig. 3.2 shows an example of why we believe an OLSDM-Pipelined hybrid might have an efficiency advantage. The figure shows a comparison between a 14-bit pipelined ADC and a 14-bit hybrid ADC. A 14-bit pipelined ADC need a sample and hold and seven 1.5-bit stages[1] if we use a 7-bit back-end ADC. The hybrid converter has 5 stages before the back-end (no sample an hold), a saving of three stages. The hybrid has two modulo resonators and a modulo integrator that result in a fifth order noise transfer function.

[1]The number of stages can be reduced if more bits are converted in each stage. This requires more comparators in each stage, a 1.5-bit pipelined stage has two comparators. The accuracy of a comparator in a B-bit stage must be $\pm V_{REF}/2^B$. Mismatch determine the accuracy of the comparators, which usually limit the number of bits per stage to 3-bits.

To clarify why we believe that OLSDM can have an advantage, we will describe some of the challenges in high-speed, high-accuracy converters. These are:

Clock skew In pipelined ADCs clock skew between the sub-ADCs and the sampling network (input switches and sampling capacitors) is a challenge. This skew (difference in delay) cause a signal dependent offset. The problem can be alleviated by placing a sample and hold before the first stage.

In the hybrid only the sampling capacitors are connected to the input. Thus, clock skew is not a problem and the hybrid does not need a separate sample and hold.

Capacitor size In a 14-bit pipelined converter with low signal swing the capacitor size can be large. For 1V peak-to-peak input swing the input capacitance has to be 53pF (from (2.7)). In 90nm CMOS this capacitance will measure 163μm by 163μm, which is a large area.

The capacitor size can be reduced by oversampling. In the hybrid example in Paper 3 the oversampling ratio is four, accordingly the sampling capacitors can be reduced by a factor of four (13pF).

Opamp DC gain is a significant challenge, and it is equivalent in the hybrid and pipelined ADC. The error introduced by finite opamp gain cause static non-linearities in a pipelined ADC—this limits the accuracy of the converter to below the gain of the first opamp.

In the hybrid the finite opamp gain cause leakage of quantization error from each modulo integrator. The error is shaped by the preceding signal transfer function. As a result, the opamp gain can be scaled differently than in a pipelined ADC.

ADC speed translate into opamp branch current. The hybrid runs four times faster than the pipelined ADC, but has four times less capacitance, which cancel with respect to current consumption. But the hybrid has a switched-capacitor circuit with at least three clock phases,

compared to two clock phases for pipelined ADC. Assuming the settling requirements are the same for the pipelined ADC and the hybrid, the hybrid opamps must be 1.5 times faster than in the pipelined ADC. Preliminary simulations suggest that the hybrid will require opamps even faster than this, but a thorough study is left for future work.

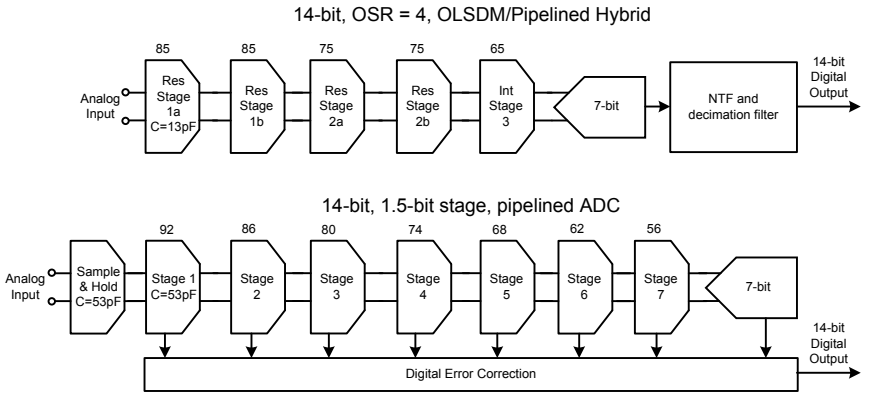

Fig. 3.2: Comparison between a 14-bit high-speed OLSDM and a 14-bit pipelined converter. The numbers above the stages denote the required operational amplifier DC gain in dB.

Paper 1: Analog Modulo Integrator For Use In Open-Loop Sigma-Delta Modulators

In this paper we introduce the switched-capacitor modulo integrator. The modulo integrator makes it possible to design an open-loop sigma-delta modulator. The theory of OLSDM and analog modulo integration is explained and verified through simulation.

Paper 2: Switched Capacitor Analog Modulo Integrator For Application In Open Loop Sigma-Delta Modulators

Paper 2 is an invited paper based on Paper 1, hence there is some overlap in the areas covered. Paper 2 discuss one of the error effects in OLSDM (false modulo) and investigate effects of a non-linear quantizer. Behavioral level

simulations in SPICE of the analog modulo integrator verify the function, and prove the concept of amplitude modulated OLSDM.

Paper 3: Resonators In Open-Loop Sigma-Delta Modulators

In Paper 3 we introduce the modulo resonator for use in open-loop sigma-delta modulators. The OLSDM presented in this work is intended for use in high accuracy (14- bit), high-speed ADCs. The modulo resonator is used with a modulo notch filter to insert a zero in the noise transfer function at a non-zero frequency. The effect of finite gain in modulo integrators and modulo resonators are described and verified through simulation. The modulo resonator and previously published modulo integrator are used in a behavioral model of a switched-capacitor fifth-order OLSDM with more than 13-bit effective number of bits for an oversampling ratio of four.

We prove for the N-order OLSDM that the number of bits in the quantizer (B) must be larger than N to ensure equivalence between OLSDM and sigma-delta modulation.

3.2 Efficient circuit solutions for pipelined ADCs

Circuit solutions that remove the opamp from switched-capacitor circuits have received interest from the research community. The idea is to replace the hard to make opamps with something more amenable to nano-scale CMOS integration. In the papers we have focused on two techniques; open-loop amplifiers, and comparator-based switched capacitor circuits. Not only are these techniques more amenable to nano-scale integration, but CBSC has been shown to have a fundamental efficiency advantage over opamp based integration [10].

We have also investigated the comparators used in the sub-ADC in the pipelined ADCs.

Paper 4: 0.8V 1GHz Dynamic Comparator In Digital 90nm CMOS Technology

This paper present simulations of a dynamic comparator in 90nm CMOS technology. It shows how 90nm CMOS technology can achieve high speed at low supply voltages.

One of the challenges in dynamic comparators is controlling the offset over process corners. As the signal swing scales down (due to supply voltage scaling) the demands on comparators in pipelined ADC become harder to fulfill, but as the paper shows, at 90nm CMOS it is quite possible to have high-speed and low supply voltage.

Paper 5: Design of a 7-bit 200MS/s, 2mW Pipelined ADC With Switched Open-Loop Amplifiers In a 65nm CMOS Technology

In this paper we present the design of a 7-bit 200MS/s pipelined ADC with switched open-loop amplifiers in a 65nm CMOS technology. As a result of turning off the open-loop amplifiers during sampling we reduce the power dissipation by 23%. The ADC achieves a SNDR of 40dB close to the Nyquist frequency, with a power dissipation of 2mW, which results in a Walden FOM of 0.13pJ/step and a Thermal FOM of 1.6fJ/step.

Paper 6: Design and Behavioral Simulation of Comparator-Based Switched Capacitor Circuits

This paper summarize some of the design equations derived in designing and debugging the chip in Paper 7. It presents a method for calculating the required parameters for comparator-based switched capacitor circuits. The parameters are capacitance (C), current (I_0), comparator delay (T_D), current source output resistance (R_o) and comparator threshold (V_{ct}). The design equations are verified with behavioral simulations in SPICE and MATLAB.

Paper 7: An 8-bit 60-MS/s 8.5mW Differential Comparator-Based Switched-Capacitor Pipelined ADC in 90nm CMOS Technology

In this paper we present the first differential comparator-based switched-capacitor (CBSC) pipelined ADC. The switched-capacitor multiplying digital-to-analog converter (MDAC) use current sources and a comparator to do charge transfer. Continuous time bootstrapped switches are used in the first stage to reduce signal dependent switch resistance. A simple calibration algorithm correct for comparator delay variation caused by the manufacturing process. Calibration reduces ramp overshoot, which dominate the non-linearity in CBSC ADCs. The ADC is produced in a 90nm low-power CMOS technology. The ADC core is 0.85mm x 0.35mm, with a 1.2V supply for the core and 1.8V for input switches. The ADC has an effective number of bits (ENOB) of 7.05-bit, and a power dissipation of 8.5mW at 60MS/s. The ADC achieves an Waldon FOM of 1.07pJ/step and Thermal FOM of 8.09fJ/step.

3.3 Clarification of contributions

All papers have been co-authored with my supervisor Trond Ytterdal. He has provided valuable questions, guidance and resources.

Two papers have been co-authored with Øystein Knauserud. During spring of 2006 he did his master thesis on OLSDM and I was his supervisor. He worked out that to do switched-capacitor OLSDM we needed a switched-capacitor modulo integrator. As such I worked on the problem found a viable implementation of a switched-capacitor modulo integrator. He provided questions and valuable insight.

Chapter 4

Paper 1

Analog Modulo Integrator For Use In Open-Loop Sigma-Delta Modulators

Carsten Wulff, Øystein Knauserud, Trond Ytterdal

In proceedings of the 24th NORCHIP Conference, 2006.
Nov. 2006 Pages 125 - 128
Digital Object Identifier 10.1109/NORCHP.2006.329259

Errata

- Section 4.4. second paragraph, 3‘rd to last line: altough → although

Abstract

A switched-capacitor analog modulo integrator is presented. This analog modulo integrator makes it possible to design an Open-Loop Sigma-Delta Modulator (OLSDM). The theory of OLSDM and analog modulo integration is explained and verified through simulation.

4.1 Introduction

Sigma-Delta modulators have become a natural choice for analog to digital conversion in applications with low to medium bandwidth and high resolution. They are used in applications from high resolution instrumentation systems to ADSL communication systems. The purpose of the Sigma-Delta modulator is to shape the quantization error such that the spectral density of the quantization noise is non-uniform, the quantization error can for example be high-pass or bandpass filtered.

The Low-pass Conventional Sigma-Delta Modulator (LC-SDM) in its simplest form consists of an integrator followed by a quantizer. The quantized signal is fed back to the input through a digital-to-analog converter and subtracted from the input. The transfer function of the modulator will be different for the input signal and the quantization error of the quantizer. The input signal will normally undergo an integration followed by a differentiation and have a transfer function close to one. The quantization error will be differentiated and thus high pass filtered.

Ideally this system could be implemented by an integrator followed by a quantizer and a differentiator. However, an ideal integrator has infinite DC gain, and with limited input swing in analog electronic circuits, an ideal integrator is not possible to implement. This is the reason why feedback is used, the feedback serves to limit the signal swing.

Another approach to sigma-delta modulators is the Frequency Sigma-Delta Modulator (FSDM) [9]. Here an amplitude to frequency modulator was used instead of an integrator, similar to what was suggested in [11]. It was shown in [9] that the preprocessing in FSDM is equivalent to modulo integration.

In [12] they introduced the non-feedback Sigma-Delta digital-to-analog converter. Here the integrator was implemented as a digital modulo integrator.

This paper introduces an analog modulo integrator for use in OLSDM. The outline of this paper is as follows. Section 4.2 explains that OLSDM are mathematically equivalent to LC-SDM. In Section 4.3 the analog switched-capacitor modulo integrator is presented, to our knowledge, it is the first of

its kind. System simulations in Section 4.4 of the OLSDM verify the theory.

4.2 Open Loop Sigma-Delta Modulator

4.2.1 Proof of Equivalence

The equivalence of LC-SDM and OLSDM was shown in [12]. We endeavor to explain the equivalence in a more intuitive way.

The OLSDM has been modeled as a quasi-linear system. Quasi-linear since the modulo integration and modulo differentiation are stepwise linear. The quantizer has been modeled as a linear addition of noise. Figure 4.1 shows the complete modulator. It should be noted that this system is similar to the system presented in Figure 1 in [11], but they used a form of FM modulation to implement the modulo integration.

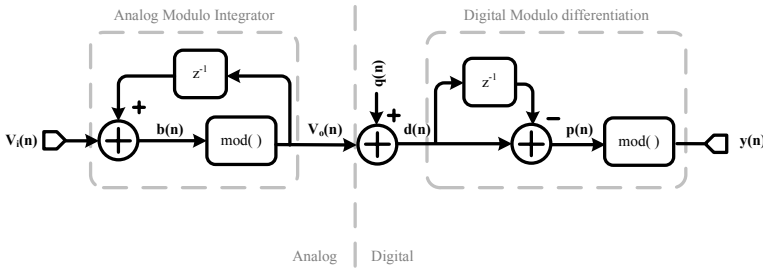

Figure 4.1: Quasi-linear model of OLSDM

We define the previous output from the integrator as

$$V_o(n-1) \in \langle -V_{ref}, V_{ref} \rangle \tag{4.1}$$

and the input signal as

$$V_i(n) \in \langle -V_{ref}, V_{ref} \rangle \tag{4.2}$$

where V_{ref} is the reference voltage.

We know that after integration, but before the modulo operation, we get

$$b(n) = V_i(n) + V_o(n-1) \tag{4.3}$$

where $b(n)$ will be bounded by

$$b(n) \in \langle -V_r, V_r \rangle \tag{4.4}$$

where $V_r = 2V_{ref}$. The modulo operation is used to reduce the output swing to $V_o(n) \in \langle -V_{ref}, V_{ref} \rangle$. The modulo operation subtracts or adds V_r, depending on the value of the summation in (4.3). The next output from the integrator can be written as

$$V_o(n) = \begin{cases} b(n) + V_r & b(n) \in \langle -V_r, -V_{ref}] \\ b(n) & b(n) \in \langle -V_{ref}, V_{ref} \rangle \\ b(n) - V_r & b(n) \in [V_{ref}, V_r \rangle \end{cases} \tag{4.5}$$

After quantization the input to differentiation will be

$$\begin{aligned} d(n) &= V_o(n) + q(n) \\ d(n-1) &= V_o(n-1) + q(n-1) \end{aligned} \tag{4.6}$$

where $q(n), q(n-1)$ are the quantization errors. The the output of the differentiator is

$$z(n) = d(n) - d(n-1) \tag{4.7}$$

If we in (4.7) insert for $d(n)$, $d(n-1)$, $V_o(n)$ and set $e(n) = q(n) - q(n-1)$ the expression becomes

$$z(n) = \begin{cases} V_i(n) + V_r + e(n) & V_i(n) \in \langle -V_{ref}, 0 \rangle \\ V_i(n) + e(n) & V_i(n) \in \langle -V_{ref}, V_{ref} \rangle \\ V_i(n) - V_r + e(n) & V_i(n) \in \langle 0, V_{ref} \rangle \end{cases} \tag{4.8}$$

Thus, the output of the modulator is

$$y(n) = \begin{cases} V_i(n) + V_r - V_r + e(n) \\ V_i(n) + e(n) \\ V_i(n) - V_r + V_r + e(n) \end{cases} \tag{4.9}$$

and for all cases in (4.9), $y(n) \in \langle -V_{ref}, V_{ref} \rangle$, if we ignore the quantization

error. This gives us the well known equations

$$\frac{y(z)}{V_i(z)} = 1\,,\ \frac{y(z)}{q(z)} = 1 - z^{-1} \tag{4.10}$$

The transfer function from the input signal to the output is one, which is the same as for a LC-SDM (often the transfer function of a LC-SDM from input to output contains a time delay, $y(z)/V_i(z) = z^{-1}$). The quantization error is differentiated, thus first order high pass filtered. This proof can be extended to higher order modulators.

4.3 The Analog Modulo Integrator

As shown, the modulo integrator is an integrator that resets when the output increases or decreases beyond a reference voltage. It keeps the remainder that exceeds the reference voltage. A requirement set on the analog modulo integrator is that it should use maximum swing available, for example 0.8V peak-to-peak with 1.2V supply. It should also be a discrete time system. The discrete time equation for a modulo integrator was shown in (4.5).

Using pseudo code the modulo integrator can be described as

1. Add the previous output to the current input
2. If the new output exceeds the reference voltages
3. Subtract/Add the range of the integrator, V_r
4. Set the current output to the remainder

This is trivial to implement in the digital domain, but it may not be obvious how it should be implemented in the analog domain. Adding two voltages in the analog domain is conceptually trivial. Whether a voltage exceeds a reference can be detected using a comparator. Subtraction in the analog domain is also trivial, but keeping the remainder presents a challenge.

Assume that the reference voltages are symmetric around the common mode, such that $|V_{ref}| = |-V_{ref}|$ and $|V_{ref}| + |-V_{ref}| = V_r$. The maximum voltage would be less than $V_{ref} + V_{ref} = V_r$ or more than $-V_{ref} + -V_{ref} =$

$-V_r$. So the output after summation, but before modulo operation, will be bounded by

$$-V_r < b(n) < V_r \tag{4.11}$$

In a circuit where the analog value is represented by voltages the swing would have to be $2V_r$ to accuratly represent all analog values. Since our input signal has a range of V_r we would waste an extra range of V_r just to represent intermittent values in the integrator. It would be best if we could set the voltage swing of the circuit to V_r, which is equal to the maximum input swing. But in a circuit where the analog values are represented with voltages this is difficult.

4.3.1 A Solution Based on Switched Capacitors

Switched-Capacitor (SC) circuits are prevalent in many analog integrated circuits. In discrete time Sigma-Delta modulators it is common to implement the integrator with a switched-capacitor circuit. It turns out that with small modifications a switched-capacitor integrator can be converted to an analog modulo integrator.

Realizing that in a switched capacitor integrator the analog value is stored as charge and not as voltages is the key to understanding how a modulo integrator can be implemented. A conventional switched-capacitor integrator, shown in Figure 4.2, adds the previous output and current input. When the integrator has settled, or failed to settle due to saturation of the opamp, it can be detected whether the output voltage exceeds the reference voltage. If it does exceed, a charged capacitor is connected to the charge transfer node of the integrator, node V_g in Figure 4.2. This subtracts/adds the charge which represent V_r. Provided that the input signal to the integrator never exceeds positive or negative reference, the subtracted/added charge will bring the integrator back within bounds. Since the analog information is stored in charge, the remainder is conserved.

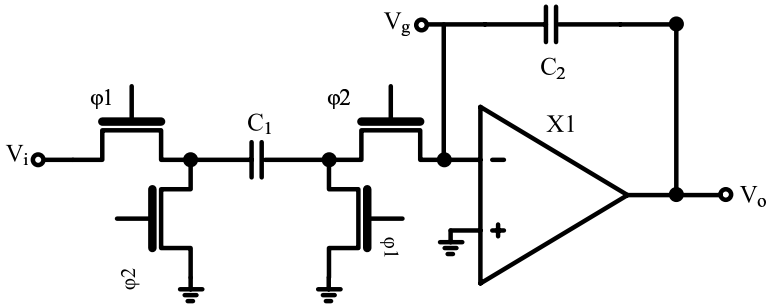

Figure 4.2: Conventional Switched-Capacitor Integrator

4.3.2 Equations of the SC Modulo Integrator

The circuit needed to implement a modulo integrator is shown in Figure 4.3. It is connected to integrator in node V_g and V_o. The complete circuit has three clock phases; $\phi 1$, $\phi 2$ and $\phi 3$. The timing diagram is shown in Figure 4.4, where T denotes the period.

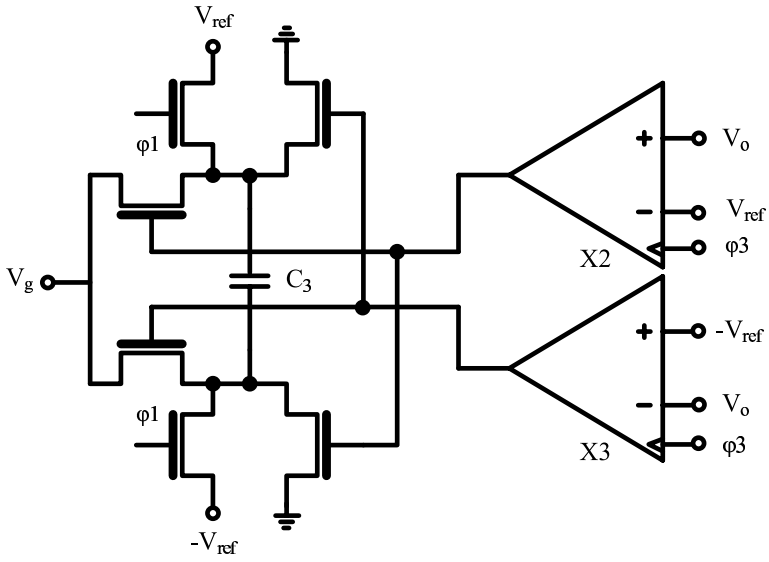

Figure 4.3: Modulo circuit

Consider the integrator in Figure 4.2, during clock phase $\phi 1$ the input signal is sampled across capacitor C1. In clock phase $\phi 2$, before $\phi 3$, the

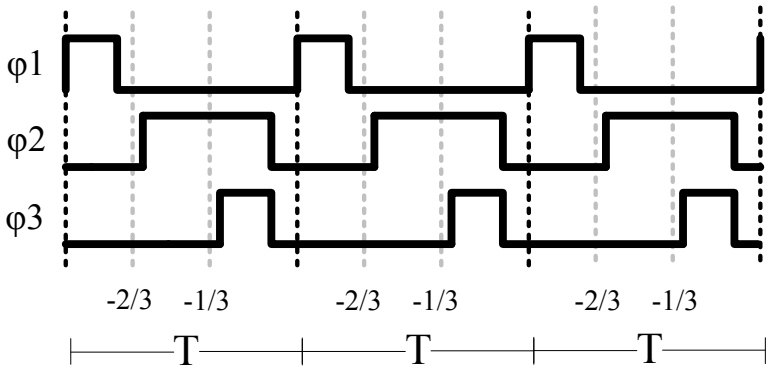

Figure 4.4: Timing diagram for the modulo integrator

charge from C1 is transfered to C2. The charge transfer equation will be

$$C_2V_o(n-T/3) = C_2V_o(n-T) + C_1V_i(n-2T/3) \tag{4.12}$$

In this equation the output, $V_o(n-T/3)$, is equivalent to $b(n)$ from (4.3) and will have the same bounds, assuming $C_1 = C_2$. To make sure that the final output, $V_o(n)$, stays within the reference voltages, V_r has to be added or subtracted as in (4.5).

To perform the addition/subtraction the circuit in Figure 4.3 is used. The different states of this circuit are shown in Figure 4.5. During $\phi 1$, Figure 4.5 a), the capacitor C_3 is charged to $V_r = V_{ref} - -V_{ref}$. During $\phi 3$ the latched comparators ($X2$ and $X3$ in Figure 4.3) determine whether the output voltage exceeds the reference. Figure 4.5 b) shows the connections if the output voltage, $V_o(n-T/3)$, is higher than V_{ref}. Here a charge of $Q_3 = C_3V_r$ is transfered to the node V_g in the integrator. This will change the charge transfer equation into

$$C_2V_o(n) = C_2V_o(n-T) + C_1V_i(n-2T/3) - C_3V_r \tag{4.13}$$

For $V_o(n-T/3)$ lower than $-V_{ref}$, Figure 4.5 c), the polarity of the charge is reversed and the charge transfer function is

$$C_2V_o(n) = C_2V_o(n-T) + C_1V_i(n-2T/3) + C_3V_r \tag{4.14}$$

And if $-V_{ref} < V_o(n - T/3) < V_{ref}$ the capacitor C_3 is not connected to V_g and the charge transfer function (4.12) remains unchanged. Notice that the outputs from the comparators can never be high at the same time, because $V_o(n - T/3)$ cannot be higher than V_{ref} and lower than $-V_{ref}$ at the same time.

Combining the three equations, (4.12), (4.13) and (4.14) with $C_1 = C_2 = C_3$ and ignoring the frational timesteps ($n - T/3$ and $n - 2T/3$) the result is (4.5).

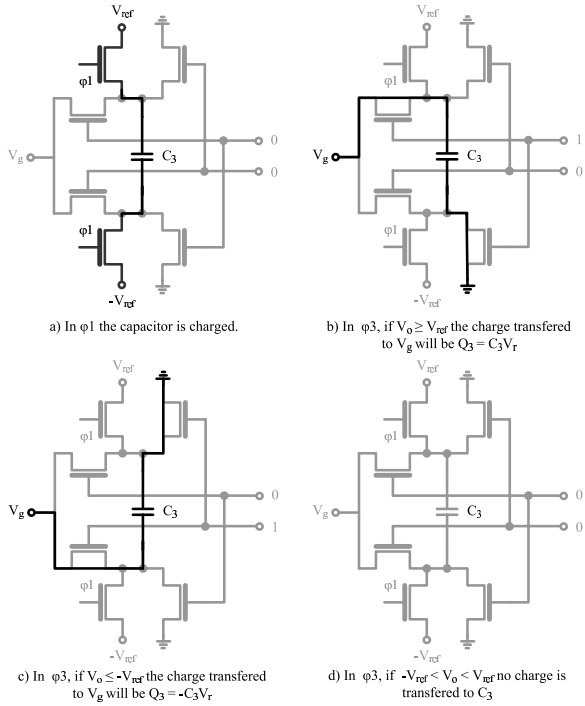

Figure 4.5: The different permutations of the modulo circuit

4.3.3 Simulation of the SC modulo integrator

Simulation of the SC modulo integrator have been performed in AimSPICE [13] using ideal models for comparators, switches and operational amplifier.

In Figure 4.6 a DC input signal $V_i = 0.3V$ was used, the reference voltages were set to 1V. At around 5μ the integrator resets, here the output

value would be $1.2V$ if it was not reset, and we can clearly see that the remainder is conserved

$$-1V + 0.2V = -0.8V \tag{4.15}$$

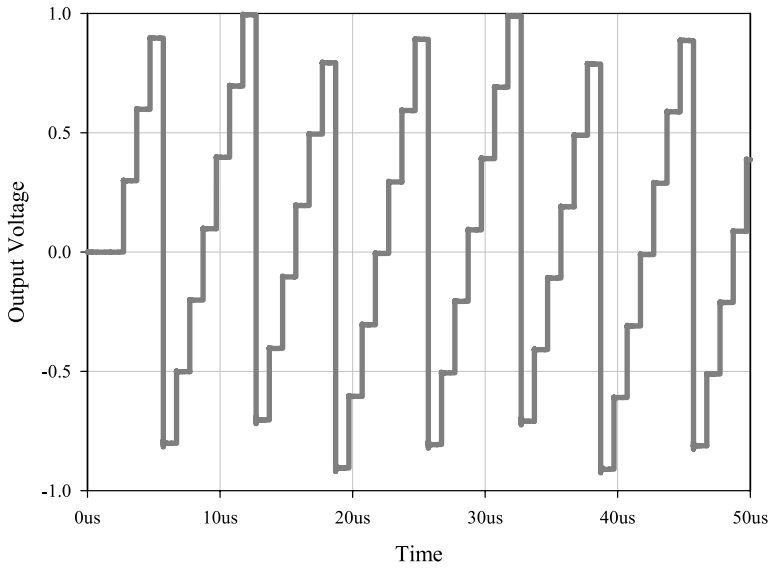

Figure 4.6: Input vs output for the modulo integrator with constant input $V_i = 0.3V$

In Figure 4.7 the input and output for a sinusoidal input to the analog modulo integrator is shown. The reference voltage, V_{ref}, was set to 1V. The sinusoidal input had an amplitude of $0.99V$. The output has been sampled at the end of $\phi 3$ and it can be seen how it never exceeds the references at V_{ref} and $-V_{ref}$.

4.4 Simulation of OLSDM Modulator

The OLSDM was modeled in SystemDotNet [14], which is a mixed-signal discrete-time event driven simulator. A third order OLSDM with 8 bit quantizer was modeled. The spectral density plot can be seen in Figure 4.8. From the plot we can clearly see that we have third order high-pass

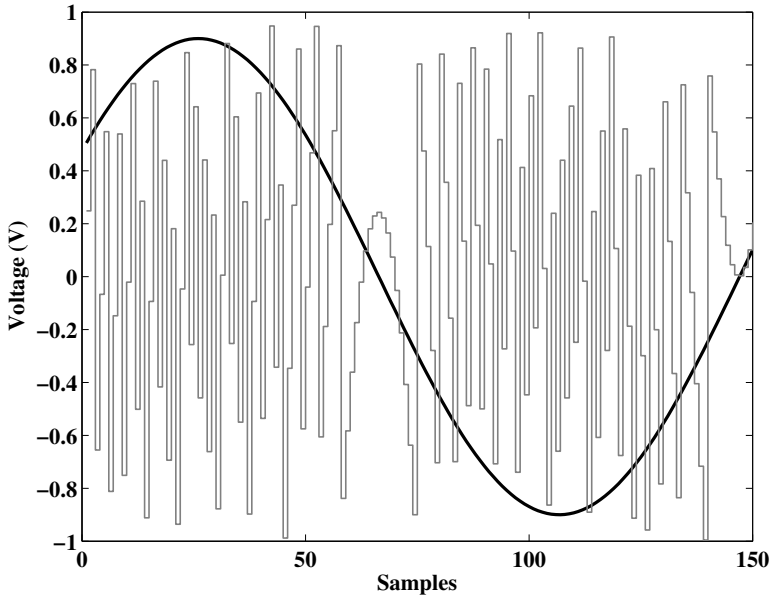

Figure 4.7: Input vs output for the modulo integrator. Input is a sine with an amplitude of 0.99 V

filtering of the quantization noise since the slope of the noise floor is 60dB per decade. The dark-gray plot is an oversampled quantizer without noise shaping, shown for comparison. With an oversampling ratio of eight we get an ENOB (Effective Number Of Bits) of 15 bits. With just oversampling, no noise shaping, we get an ENOB of 9.5 bits.

The analog modulo integrator can be compared to a first order, 1.5 bit LC-SDM. In Figure 4.9 we have plotted the output from the OLSDM and the combined outputs from the comparators in the analog modulo integrator (outputs of X2 and X3 in Figure 4.3). We can clearly see that the combined output of the comparators is a first order noise shaped version of the input signal. One could summize that the analog modulo integrator is just a 1.5 bit LC-SDM, but that would be inaccurate. If we assume the input signal is bounded by (4.2), the analog modulo integrator output will never exceed $-V_{ref}$ or V_{ref}, altough the output during $\phi 2$ might saturate. For the LC-SDM the input signal swing is normally reduced such that the output of the integrator does not saturate.

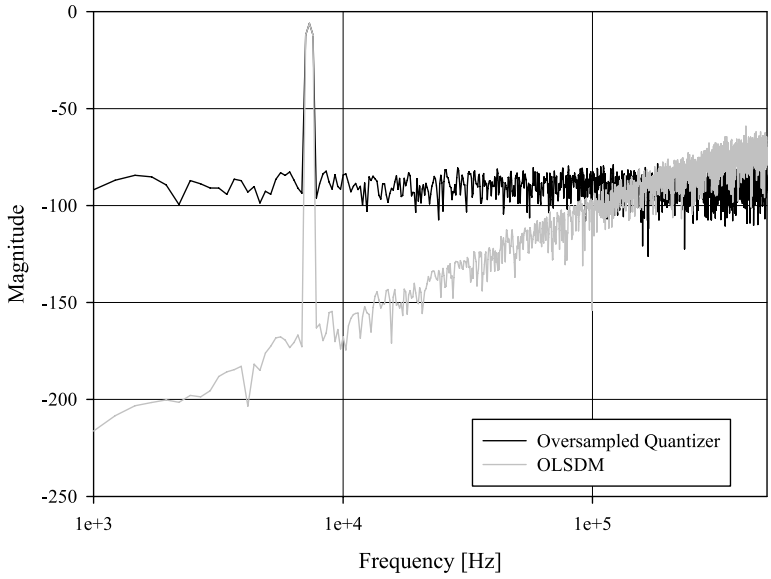

Figure 4.8: Simulation of third order, 8 bit OLSDM. Input signal amplitude is 0.5 and sampling frequency is 1MHz. Also shown is the output from a oversampled quantizer without noise shaping

4.5 Future Work

The OLSDM architecture with analog modulo integrator is, to our knowledge, a new architecture. Thus there are many questions to be answered and some questions that have not yet been asked. Research is currently being performed on the effects of mismatch, finite opamp gain, non-linearity of quantizer, finite number of bits in quantizer, and effects of parasitics. We hope to have an answer to some of these questions in the near future.

4.6 Conclusion

A switched-capacitor analog modulo integrator was presented. This analog modulo integrator made it possible to design an Open-Loop Sigma-Delta Modulator (OLSDM). The theory of OLSDM and analog modulo integration was explained and verified through simulation.

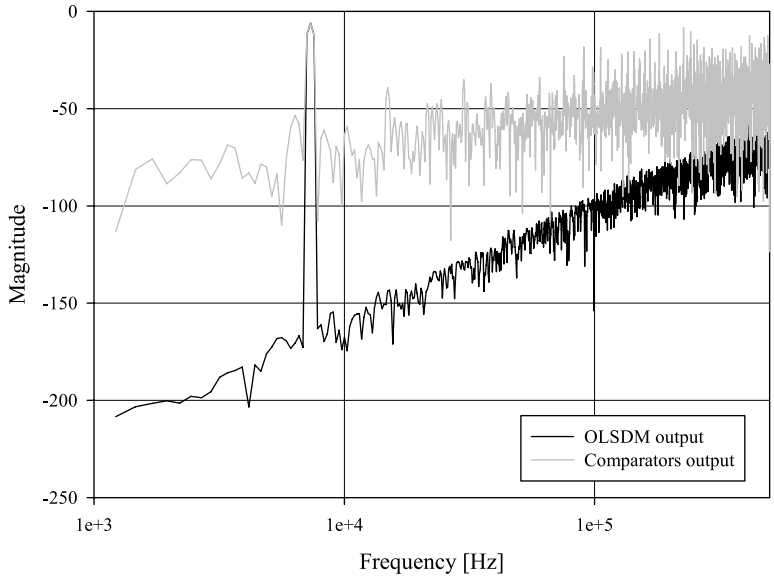

Figure 4.9: The combined output of the comparators and the output of the OLSDM

Acknowledgments

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Chapter 5

Paper 2

Switched Capacitor Analog Modulo Integrator For Application In Open Loop Sigma-Delta Modulators

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Errata

- Section 5.3.3, 5'th line: an → a

- Section 5.3.3, second to last paragraph: We say that quantization noise can have codes that span the range of the quantizer, but this is incorrect. Quantization noise is limited to 1LSB, so the maximum difference between two output codes with the same analog input is 1LSB. This assumes that thermal noise is less than 1LSB. Thus, the statment in the second to last paragraph is not valid for quantizers with more than on bit.

Abstract

We introduce the switched capacitor analog modulo integrator, which to our knowledge is a new circuit. We introduce the amplitude modulated open loop Sigma-Delta modulator (OLSDM), which is an analog modulo integrator followed by a quantizer and a modulo differentiator. The mathematical equivalence between low pass Sigma-Delta modulators and OLSDM is explained. Behavioral simulations confirm the equivalence. The necessary circuit, a switched capacitor analog modulo integrator, is explained in detail. Behavioral level simulations in SPICE of the analog modulo integrator verify the function, and prove the concept of amplitude modulated OLSDM.

Keywords Sigma-Delta Modulators, Switched Capacitor Circuits, Analog Modulo Integrator

5.1 Introduction

Sigma-Delta modulators have become a natural choice for analog-to-digital conversion in applications with low to medium bandwidth and high resolution. The Sigma-Delta modulator shapes the spectral density of the quantization error of data converters. The quantization error, or as it is often called, quantization noise, is the error introduced by converting a continuous value signal into a discrete value signal. This error is often considered to have uniform spectral density, or in other words, be a white noise source. The conditions for considering quantization error as a white noise source was covered in [15].

The conventional low-pass Sigma-Delta modulator (L-SDM) in its simplest form consists of an integrator followed by a quantizer. The quantized signal is fed back to the input through a digital-to-analog converter (DAC) and subtracted from the input. The transfer function of the modulator is different for the input signal and the quantization noise. [1] The input signal

[1] This assumes a linear model of the quantizer, since the transfer function is only defined for a linear system

will undergo an integration followed by a differentiation and have a transfer function of one. The quantization noise will be differentiated and thus high pass filtered.

In an ideal world, with no voltage swing limitations, an L-SDM system could be implemented by an integrator followed by a quantizer and a differentiator, but since supply voltage is limited in electronic circuits, and an integrator has infinite dc gain, it is difficult to implement. Somehow the output swing of the integrator has to be limited. Feedback is normally used to limit the output swing of the integrator.

There are many different types of Sigma-Delta modulators. In this paper we discuss a small sub group that we denote Open Loop Sigma-Delta Modulators (OLSDM). We define an OLSDM as: Any Sigma-Delta modulator that does not have feedback of the quantized modulator output signal.

One of the first suggestion of an OLSDM can be found in [11]. Although there is no system implementation they explain a method that avoids the feedback DAC. More recently there have been others like the Frequency Sigma-Delta Modulator (FSDM) in [9] and [16].

In the FSDM a voltage to frequency converter, a voltage controlled oscillator (VCO), was used in place of the integrator, and it was shown in [9] that the pre-processing in FSDM is equivalent to modulo integration. The FSDM could be identified as a frequency modulated OLSDM.

In [12] they introduced the non-feedback Sigma-Delta digital-to-analog modulator where the integrator was implemented as a digital modulo integrator.

In the past the noise shaping of Sigma-Delta modulators has been combined with the high speed of pipelined ADCs. In [7] a second order five bit Sigma-Delta Modulator was cascaded with a 12 bit pipelined ADC. The output of the Sigma-Delta Modulator was combined with the output of the pipelined ADC to generate the digital output word. We wanted to investigate whether one could avoid any interaction, with the exception of the input and output signals, between the Sigma-Delta Modulator and the pipelined ADC in such a system. The question was; could one pre-process the input signal to implement the sigma, quantize and do post-processing

to perform the delta, without interaction between the sigma and the delta. The block diagram of such a system is shown in Figure 5.1

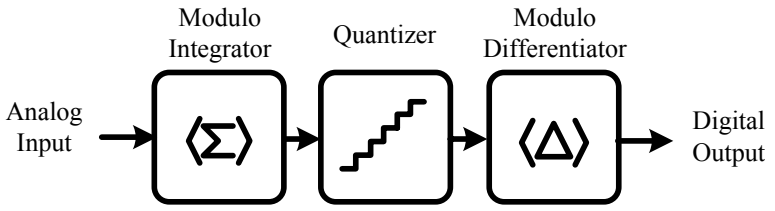


Figure 5.1: First order OLSDM block diagram

We knew from [12] that the open loop Sigma-Delta modulator was possible when all blocks were digital, by using modulo integration, quantization and modulo differentiation. However, in an analog-to-digital OLSDM the modulo integration would have to occur in the analog domain. We were unable to find any published circuit that matched our requirements for an analog modulo integrator. Accordingly, the switched capacitor analog modulo integrator was developed, which we present here. To our knowledge, this switched capacitor analog modulo integrator is a new circuit.

In Section 5.2 we elaborate on the mathematical equivalence between OLSDM and L-SDM, which is supported by behavioral simulations in Matlab in Section 5.3. Quantizer non-linearity and common errors are also discussed in Section 5.3. In Section 5.4 we introduce the analog switched capacitor modulo integrator. Behavioral level simulations with a SPICE macro model of the analog modulo integrator and the OLSDM are presented in Section 5.5.

5.2 Open Loop Sigma-Delta Modulator

The most basic low pass OLSDM is an integrator, followed by a quantizer and a differentiator as illustrated by Figure 5.1. The input signal is integrated and afterwards differentiated, hence the output is equal to the input, assuming a linear system. The quantization error added by the quantizer is differentiated thus high pass filtered. To limit the swing in the analog domain we use a modulo operation at the output of the integrator. The

inverse operation, which is also a modulo operation, is performed in the digital domain after the differentiator. A modulo operation is trivial to implement in the digital domain. The analog modulo operation is not trivial, and it has previously been implemented as a voltage to frequency converter in [9] and [16].

The equivalence of L-SDM and OLSDM was shown in [12]. Here we endeavor to explain the equivalence more intuitively.

The OLSDM has been modeled as a piecewise linear system. The modulo operation is a non-linear operation, but it can be seen as a piecewise linear system if we ignore the discontinuities when the modulo operation occurs. The quantizer has been modeled as a linear addition of noise. Figure 5.2 shows the complete modulator.

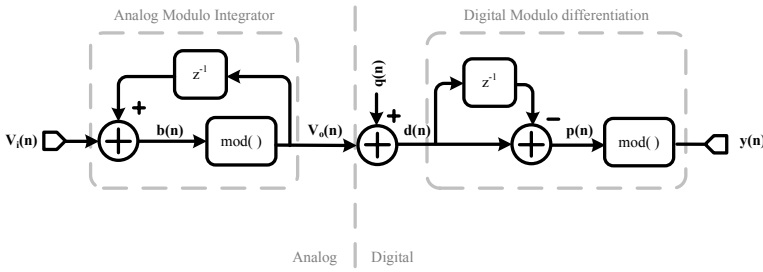


Figure 5.2: Piecewise linear model of the OLSDM

The input signal to the modulator is $V_i(n)$, where n is the sample index. A signal with sample index n is the current sample while $n-1$ is the previous sample. The input is added to the previous output of the integrator, $V_o(n-1)$, resulting in $b(n)$. The signal $b(n)$ is subjected to modulo operation with $V_o(n)$ as a result. $d(n)$ is the sum of $V_o(n)$ and the quantization noise, $q(n)$. The differentiator output $p(n)$ is $d(n)$ minus the previous quantizer output $d(n-1)$. To get the output, $y(n)$, $p(n)$ is subjected to a modulo operation. In this system the second modulo operation cancels the first modulo operation and we have a system that is equivalent to an L-SDM. The equations in more detail follow.

We define the previous output from the integrator as

$$V_o(n-1) \in \langle -V_{ref}, V_{ref} \rangle \tag{5.1}$$

and the input signal as

$$V_i(n) \in \langle -V_{ref}, V_{ref} \rangle \tag{5.2}$$

where V_{ref} is the reference voltage.

We know that after integration, but before the modulo operation, we get

$$b(n) = V_i(n) + V_o(n-1) \tag{5.3}$$

where $b(n)$ will be bounded by

$$b(n) \in \langle -V_r, V_r \rangle \tag{5.4}$$

where $V_r = 2V_{ref}$. The modulo operation is used to reduce the output swing to $V_o(n) \in \langle -V_{ref}, V_{ref} \rangle$. The modulo operation subtracts or adds V_r, depending on the value of the summation in (5.3). The next output from the integrator can be written as

$$V_o(n) = \begin{cases} b(n) + V_r & b(n) \in \langle -V_r, -V_{ref}] \\ b(n) & b(n) \in \langle -V_{ref}, V_{ref} \rangle \\ b(n) - V_r & b(n) \in [V_{ref}, V_r \rangle \end{cases} \tag{5.5}$$

Accordingly (5.5) is the equation for a modulo integrator. After quantization the input to differentiation will be

$$\begin{aligned} d(n) &= V_o(n) + q(n) \\ d(n-1) &= V_o(n-1) + q(n-1) \end{aligned} \tag{5.6}$$

where $q(n), q(n-1)$ are the quantization errors. The the output of the differentiator is

$$p(n) = d(n) - d(n-1) \tag{5.7}$$

If we in (5.7) insert for $d(n)$, $d(n-1)$, $V_o(n)$ and set $e(n) = q(n) - q(n-1)$ the expression becomes

$$p(n) = \begin{cases} V_i(n) + V_r + e(n) & V_i(n) \in \langle -V_{ref}, 0 \rangle \\ V_i(n) + e(n) & V_i(n) \in \langle -V_{ref}, V_{ref} \rangle \\ V_i(n) - V_r + e(n) & V_i(n) \in \langle 0, V_{ref} \rangle \end{cases} \tag{5.8}$$

The bounds of $V_i(n)$ in (5.8) are derived from the possible input signal values for the modulator to reach the states in (5.8). Consider the first case where

$$p(n) = V_i(n) + V_r + e(n), V_i(n) \in \langle -V_{ref}, 0 \rangle \tag{5.9}$$

Here V_r has been added, thus

$$b(n) \in \langle -V_r, -V_{ref}] \tag{5.10}$$

from (5.5). For b(n) to have these bounds

$$V_i(n) \in \langle -V_{ref}, 0 \rangle \tag{5.11}$$

and

$$V_o(n-1) \in \langle -V_{ref}, 0 \rangle \tag{5.12}$$

This is sufficient to ensure the bounds of $p(n)$ in case 1 in (5.8) are

$$p(n) \in [V_{ref}, V_r \rangle$$

Thus when we apply another modulo operation we get

$$y(n) = \begin{cases} V_i(n) + V_r - V_r + e(n) & V_i(n) \in \langle -V_{ref}, 0 \rangle \\ V_i(n) + e(n) & V_i(n) \in \langle -V_{ref}, V_{ref} \rangle \\ V_i(n) - V_r + V_r + e(n) & V_i(n) \in \langle 0, V_{ref} \rangle \end{cases} \tag{5.13}$$

and for all cases in (5.13), $y(n) \in \langle -V_{ref}, V_{ref} \rangle$. Equation (5.13) can be expanded into

$$y(n) = V_i(n) + q(n) - q(n-1)$$

Which result in the well known equations

$$\frac{y(z)}{V_i(z)} = 1\,,\ \frac{y(z)}{q(z)} = 1 - z^{-1} \tag{5.14}$$

The transfer function from the input signal to the output is one, which is the same as for an L-SDM, although often the transfer function of an L-SDM from input to output contains a time delay, $y(z)/V_i(z) = z^{-1}$. The quantization error is differentiated, thus first order high pass filtered. This proof can be extended to higher order modulators.

5.3 Behavioral Simulations In Matlab

The behavioral simulations presented here are an implementation of the equations explained in the previous section. [2]

5.3.1 First And Second Order OLSDM

A first and second order OLSDM and an oversampled quantizer without noise shaping were modeled and simulated in Matlab. The oversampled quantizer without noise shaping was included to compare ideal results with the simulated results. All quantizers were implemented as 7 bit quantizers. An oversampling ratio (OSR) of 8 was chosen. An overview of the system can be seen in Figure 5.3.

The ideal signal to noise and distortion ratio (SNDR) for the different cases are shown in Table 5.1. The ideal SNDR are based on equations from [4].

Table 5.1: Ideal SNDR for 7 bit quantizer, OSR=8

Noise Shaping	Improvement (dB)	Total (dB)
None	$10 \times \log(OSR)$	52.9
First order	$30 \times \log(OSR) - 5.17$	65.8
Second order	$50 \times \log(OSR) - 12.9$	76.1

[2] The Matlab code for the first and second order OLSDM can be downloaded from http://www.nextgenlab.net/olsdm

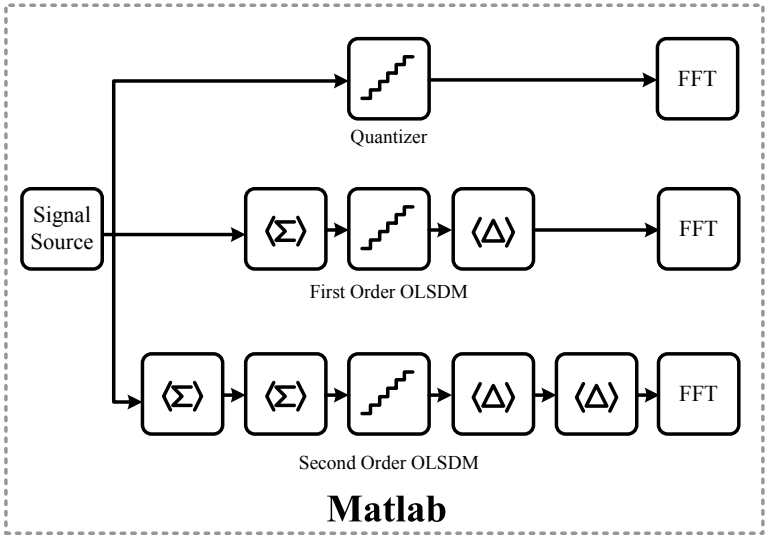


Figure 5.3: Overview of behavioral level simulation system

The equations for the OLSDM were implemented as specified in the previous section with one exception. We chose to implement the quantizer using unsigned integer outputs, the output ranging from 0-127. With this implementation $d(n)$ has a dc offset. The differentiator is a high pass filter and removes this dc offset. For the modulo operation to work, a dc offset was added after the differentiator to restore the correct common mode. In the second order OLSDM a dc offset was added after both differentiators.

The sampling frequency was chosen arbitrarily at 1MHz and the input signal was chosen according to the rules of coherent sampling [17]. In Matlab the sampling frequency is of no importance, we could just as well have used normalized frequencies. However, these simulations will be compared to SPICE simulations, and in SPICE the sampling frequency is of importance. The input frequency was $f_{in} = 6164.6Hz$ and 2^{15} samples of the output, $y(n)$, were calculated.

The input signal to the OLSDM must be limited, as specified in equation (5.2). It turns out that (5.2) is incorrect when we deal with a finite resolution quantizer, which we will discuss in the next section. For the remainder of this paper the input signal amplitude has been fixed at 0.9FSR, unless

otherwise specified. As a consequence SNDR will be 0.91dB lower than ideal cases in Table 5.1.

The outcome of simulations are summarized in Table 5.2. Both the second order OLSDM and the first order OLSDM have approximately the same SNDR as the ideal modulators. When we remove the effects of reduced input amplitude we are left with an error of $+0.2dB$ for no noise shaping, $+0.01dB$ for first order OLSDM, and $-0.19dB$ for second order OLSDM, which is within the errors of the SNDR extraction.

The Fast Fourier Transform was used to extract the SNDR, the FFTs can be seen in Figure 5.4 and Figure 5.5. The light gray spectrum in the figures are the FFTs of the ideal 7 bit quantizer, which is the same for the two figures.

Table 5.2: SNDR of OLSDM modulators with 2^{15} point FFT

Noise Shaping	Total (dB)	Difference from Ideal (dB)
None	52.2	-0.7
First order	64.9	-0.9
Second order	74.9	-1.1

5.3.2 Input Signal Amplitude Limitations

In the derivation of (5.2) we ignored quantization noise. But when we deal with a finite resolution quantizer, quantization noise cannot be ignored. With quantization noise (5.8) becomes

$$p(n) = \begin{cases} V_i(n) + V_r + e(n) & V_i(n) + e(n) \in \langle -V_{ref}, 0 \rangle \\ V_i(n) + e(n) & V_i(n) + e(n) \in \langle -V_{ref}, V_{ref} \rangle \\ V_i(n) - V_r + e(n) & V_i(n) + e(n) \in \langle 0, V_{ref} \rangle \end{cases} \tag{5.15}$$

The boundaries of (5.15) now include the quantization noise. For example for case two, where

$$p(n) = V_i(n) + e(n)$$

no digital modulo should be performed. To make certain no digital modulo

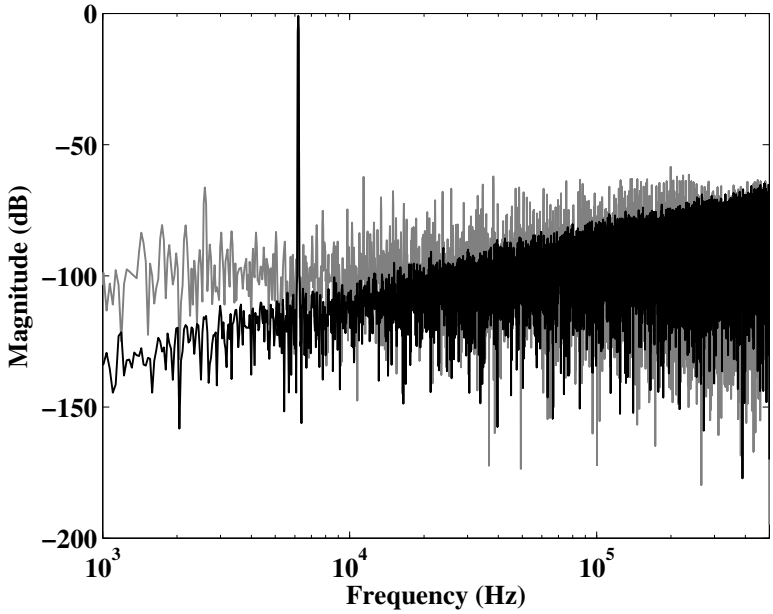


Figure 5.4: 2^{15} point FFT of the first order OLSDM output

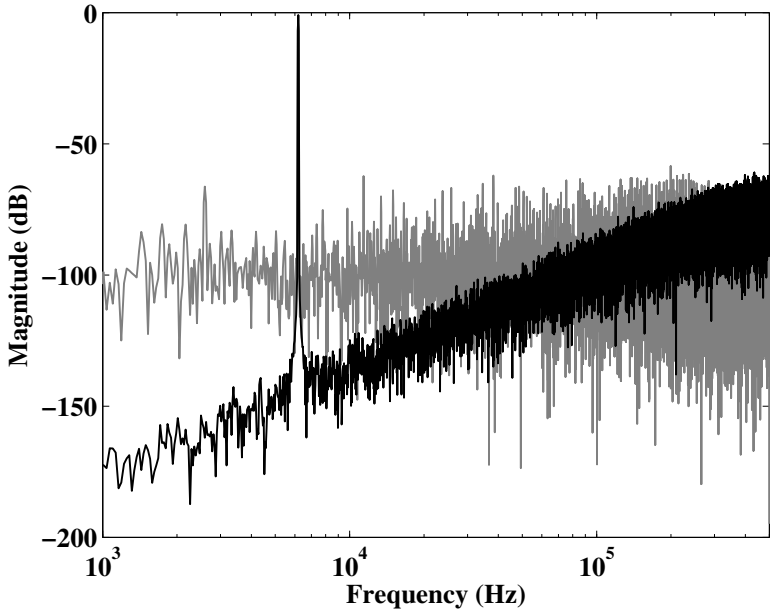


Figure 5.5: 2^{15} point FFT of the second order OLSDM output

is performed

$$V_i(n) + e(n) \in \langle -V_{ref}, V_{ref} \rangle$$

accordingly

$$V_i(n) \in \langle -V_{ref} + |e(n)|, V_{ref} - |e(n)| \rangle \tag{5.16}$$

If the input amplitude is not limited as specified by (5.16), we get a condition we denote as *false modulo* errors. For example, assume that for case two in (5.15) we get

$$p(n) = V_i(n) + e(n) <= -V_{ref} \tag{5.17}$$

as a consequence

$$y(n) = V_i(n) + V_r + e(n) \tag{5.18}$$

here a modulo operation was carried out on $p(n)$ when it should not have been.

The limit in (5.16) indicate that low resolution quantizers may not be suited for this type of OLSDM.

These errors are easy to spot in the output of the OLSDM, shown in Figure 5.6. They cause large glitches which span the range of the output codes. To avoid these errors it is sufficient to limit the input signal. It should be noted that the presence of these errors completely removes the noise shaping of the OLSDM.

In the circuit implementation of the analog modulo integrator, described by equation (5.5), we use comparators to detect $b(n) \in \langle -V_r, -V_{ref}]$ and $b(n) \in [V_{ref}, V_r \rangle$. If we use the outputs from these comparators we can prevent the *false modulo* errors from occuring. In the first order OLSDM we know that a modulo should only be performed after differentiation when a modulo was performed in the analog modulo integrator. Consequently we can use the outputs of the comparators in the modulo integrator to control the modulo operation in the differentiator. This ensures that *false modulo* errors never occur. The solution comes at the cost of delay lines that must be added to synchronize the comparator outputs from the modulo integrators

with the modulo differentiator. For the remainder of the paper we do not use this solution. In Section 5.3.3 we describe an error correction technique that corrects *false modulo* errors without using the comparator outputs.

Unrelated to these errors it was shown in [18] that for digital-to-analog OLSDM $N+1$ quantizer bits are normally needed, where N is the OLSDM order. Thus for a second order OLSDM we would need a 3 bit quantizer. We expect the same to be true for analog-to-digital OLSDM.

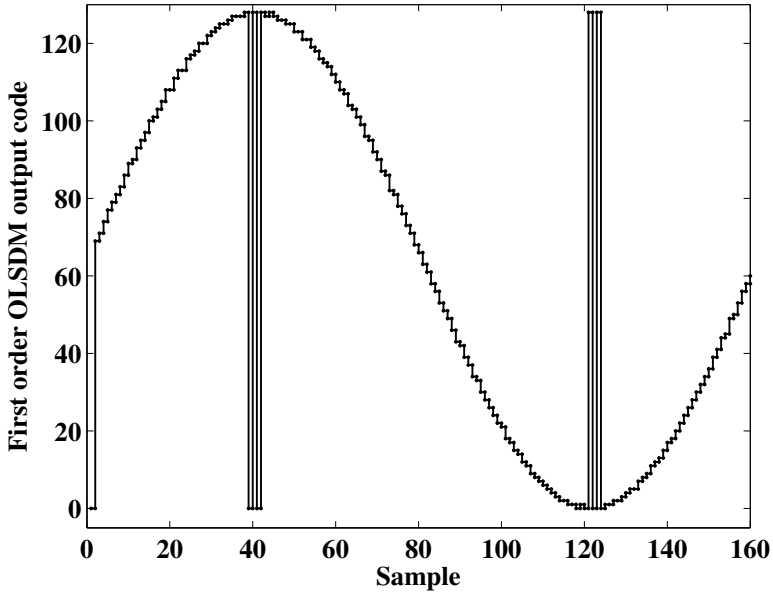


Figure 5.6: The output of the first order OLSDM in the presence of *false modulo* errors

5.3.3 Quantizer Linearity And Correction Of False Modulo Errors

An important issue of the amplitude modulated OLSDM is how the linearity of the quantizer affects the system. The step sizes in the quantizer were made dependent on the input signal, thus introducing a non-linearity. By changing the dependence on the input signal we control the linearity of the quantizer. In this example an 7 bit quantizer with a maximum of 6.8 bit linearity was used as the quantizer in the second order OLSDM. The results are

presented for two different input amplitudes, $0.8FSR$ and $0.9FSR$. Figure 5.7 shows the linearity of the OLSDM as a function of quantizer linearity. As expected, the linearity of the OLSDM does depend on the linearity of the quantizer. For each bit of reduction in the linearity of the quantizer the second order OLSDM looses half a bit of linearity. The slope is constant until a threshold is reached, the threshold marks the onset of *false modulo* errors. Below this threshold the SNDR of the OLSDM degrades rapidly. The threshold is highly dependent on the input amplitude and is on the order of (5.16). Such a sharp decrease in SNDR at a particular input signal amplitude is undesirable, and it would be advantageous to correct for the cause of the sharp degradation, the *false modulo* errors. As mentioned we can use the comparator output from the analog modulo integrators to control modulo differentiation, which will remove the *false modulo* errors. However, there is an alternate solution.

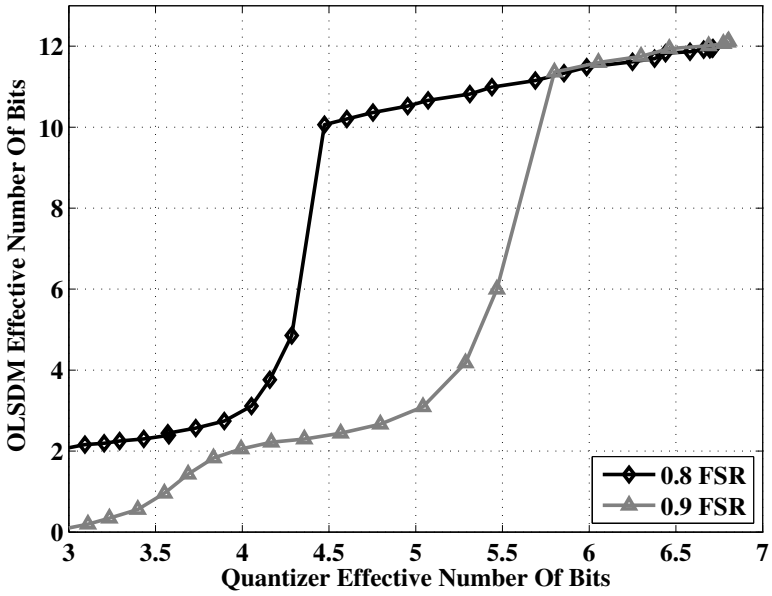


Figure 5.7: Linearity of second order OLSDM as a function of quantizer linearity

The *false modulo* errors have a large amplitude and high frequency, as seen in Figure 5.6. They span the range of the output codes in two samples,

and thus have a frequency close to the Nyquist frequency. If we take advantage of the fact that the input signal is, by choice, at least eight times lower than the Nyquist frequency, since we chose an OSR of eight, we can reduce the errors. There is a maximum difference between two adjacent output codes, which depend on the input signal. We assume a sinusoidal input at one-eight of the Nyquist frequency. A sinusoid has a maximum slope at the zero crossing which is approximately given by

$$Slope \approx A\pi/OSR \tag{5.19}$$

, where A is the amplitude. In (5.19) we have used the well known assumption that $\sin x \approx x$ if x is small and that $OSR = f_s/2f_{in}$. With an OSR of eight $Slope \approx 0.39$ at zero crossing, which is approximately one fifth of the FSR.

We assume that any change in the output of more than $0.6FSR$ between two consecutive samples is due to a *false modulo* error. If two consecutive samples of the OLSDM output has a difference of more than 0.6FSR we undo the modulo operation. The result of this simple correction can be seen in Figure 5.8. The error correction compensates for the dependence on input signal amplitude and the onset of *false modulo* errors. It should be noted that this error correction technique now allows the input signal amplitude to be FSR.

In this error correction technique we have made an assumption on the properties of the output signal of the modulator. In this assumption we must be cautious of the quantization noise. If we use a low resolution quantizer the quantization noise power at higher frequencies can be significant, and output codes which span the range of output codes in two samples are certainly possible. Having said that, with higher resolution quantizer and low order noise shaping the quantizer noise power is not significant enough to influence the error correction.

The circuit implementation of an amplitude modulated OLSDM requires an analog modulo integrator. The next section explains how such a function can be implemented by a switched-capacitor circuit.

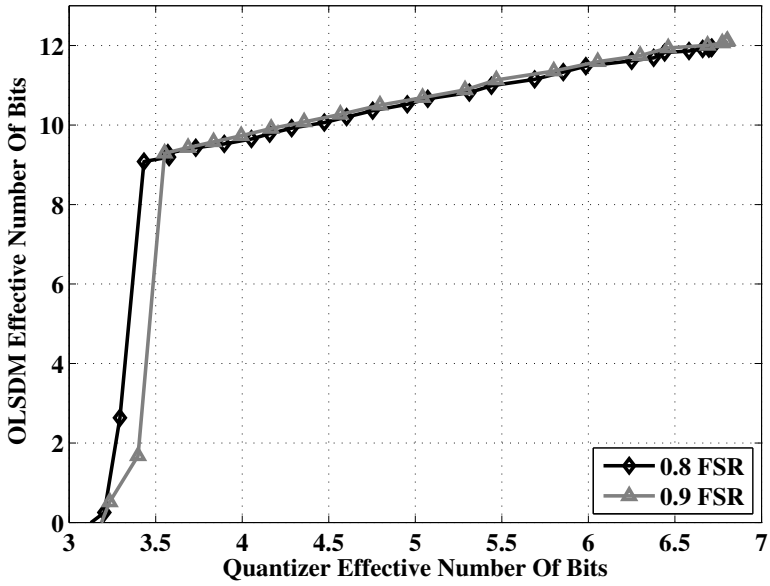


Figure 5.8: Linearity of second order OLSDM as a function of quantizer linearity with error correction enabled

5.4 The Analog Modulo Integrator

A requirement set on the analog modulo integrator was that it should use maximum swing available, for example 0.8V peak-to-peak with 1.2V supply. It should also be a discrete time system and it should be amplitude modulated and not frequency modulated as was used in [9] and [16]. The discrete time equation for a analog modulo integrator was shown in (5.5).

Using pseudo code the modulo integrator can be described as

1. Add the previous output to the current input
2. If the new output is equal to or exceeds the reference voltages
3. Subtract/Add the range of the integrator, V_r
4. Set the current output to the remainder

A modulo operation is trivial to implement in the digital domain, but it may not be obvious how it should be implemented in the analog domain.

Adding two voltages in the analog domain is conceptually trivial. Whether a voltage exceeds a reference can be detected using a comparator. Subtraction in the analog domain is also trivial, but keeping the remainder presents a challenge.

Assume that the reference voltages are symmetric around the common mode, such that $|V_{ref}| = |-V_{ref}|$ and $|V_{ref}|+|-V_{ref}| = V_r$. The maximum internal voltage in the modulo integrator would be less than $V_{ref}+V_{ref} = V_r$ or more than $-V_{ref} + -V_{ref} = -V_r$. So the output after summation, but before modulo operation, will be bounded by

$$-V_r < b(n) < V_r \tag{5.20}$$

In a circuit where the analog value is represented by voltages the swing would have to be $2V_r$ to accurately represent all analog values. Since our input signal has a range of V_r we would waste an extra range of V_r just to represent intermittent values in the integrator. It would be better if we could set the voltage swing of the circuit to V_r, which is equal to the maximum input swing. But in a circuit where the analog values are represented with voltages this is difficult.

5.4.1 A Solution Based On Switched Capacitors

Switched-Capacitor (SC) circuits are prevalent in many analog integrated circuits. In discrete time Sigma-Delta modulators it is common to implement the integrator with a switched-capacitor circuit. It turns out that with small modifications a switched-capacitor integrator can be converted to an analog modulo integrator.

In switched-capacitor circuits the analog values are represented by voltages across charged capacitors. A conventional switched-capacitor integrator, shown in Figure 5.9, adds the previous output and current input.

This simple integrator has two phases, sample ($\phi 1$) and charge transfer ($\phi 2$). Assume the charge stored on C_2 is zero ($Q_2 = 0$). In the sample phase we charge C_1 to the input voltage, thereby placing a charge of $Q_1 = V_i C_1$ on the capacitor. During charge transfer the charge of C_1 is transferred to

C_2 by forcing the voltage V_g to be equal to ground using an operational amplifier. The voltage across C_1 is then zero and there is no charge stored across it, all charge is across C_2. This causes the output voltage to be $V_o(n) = Q_1/C_2$. If the input value is kept constant, the next output value, after a clock cycle, will be $V_o(n+1) = 2Q_1/C_2$.

In the charge transfer phase V_g is a high impedance node, thus the total charge, Q_{tot}, given by $Q_{tot} = Q_1 + Q_2$, does not change. Q_{tot} is independent of the voltages at V_g and V_o. Thus we can argue that the ideal output value, $V_{o-ideal} = Q_{tot}/C_2$ is only dependent on the total charge across the capacitors. By ideal output voltage $V_{o-ideal}$ we mean the output voltage V_o if V_g was forced to ground.

A real world operational amplifier will normally have a maximum output signal swing. For example, if we exceed this signal swing the gain in the operational amplifier goes down, and it is unable to force virtual ground. In this case V_o saturates, it cannot go any higher, hence $V_o < V_{o-ideal}$. This saturation voltage we define as $V_{sat} > V_{ref}$.

Assume that the operational amplifier saturates in $\phi 2$, hence $V_o = V_{sat} > V_{ref}$. If we can detect this condition, $V_o > V_{ref}$, we can subtract a charge from V_g that represents V_r ($V_r = 2V_{ref}$ as defined in Section 5.2), thus perform a modulo operation. We would now have

$$V_{o-ideal} = (Q_{tot} - Q_{V_r})/C_2 < V_{ref} < V_{sat}$$

as a consequence the operational amplifier will be able to force virtual ground.

One of the differences between the switched capacitor analog modulo integrator and the conventional integrator is that the latter has three clock phases. The first two have the same function as in the conventional integrator, sample and charge transfer. The third clock phase is added to detect if $V_o > V_{ref}$ (and the opposite, $V_o < -V_{ref}$) in phase two. If it does exceed, a charged capacitor is connected to the charge transfer node of the integrator, node V_g in Figure 5.9. This subtracts or adds the charge which represent V_r. This will change the charge transfer equation, and as we shall see, implement a modulo operation.

Provided that the input signal limited as specified by (5.16), the subtracted/added charge will ensure that

$$-V_{ref} < V_o < V_{ref} \tag{5.21}$$

The circuit needed to implement a modulo integrator is shown in Figure 5.10. It is connected to the integrator in node V_g and V_o. The complete circuit has, as mentioned, three clock phases; $\phi 1$, $\phi 2$ and $\phi 3$. The timing diagram is shown in Figure 5.11, where T denotes the period and $1/3, 2/3$ denotes the fractional time steps.

Consider the integrator in Figure 5.9. During clock phase $\phi 1$ the input signal is sampled across capacitor C1. In clock phase $\phi 2$, before $\phi 3$, the charge from C1 is transferred to C2. The charge transfer equation will be

$$C_2 V_o(n - T/3) = C_2 V_o(n - T) + C_1 V_i(n - 2T/3) \tag{5.22}$$

In this equation, $V_o(n - T/3)$, is equivalent to $b(n)$ from equation (5.3) and will have the same bounds, assuming $C_1 = C_2$. For the output, $V_o(n)$, to stay within the reference voltages, V_r has to be added or subtracted as in equation (5.5).

Figure 5.12 shows the states of Figure 5.10 in more detail. During $\phi 1$, Figure 5.12 a) , the capacitor C_3 is charged to $V_r = V_{ref} - -V_{ref}$. At the start of $\phi 3$ the latched comparators ($X2$ and $X3$ in Figure 5.10) determine whether the output voltage exceeds the reference. Figure 5.12 b) shows the

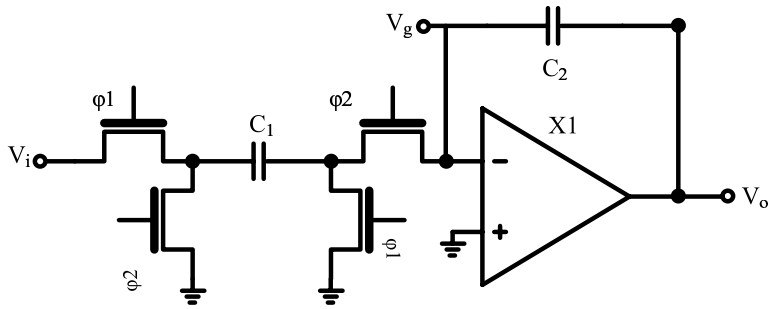


Figure 5.9: Conventional switched capacitor integrator

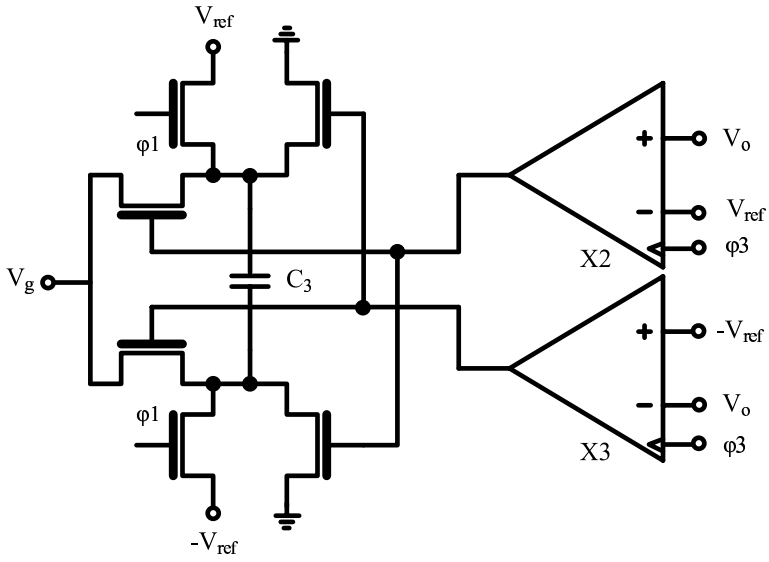


Figure 5.10: Modulo circuit

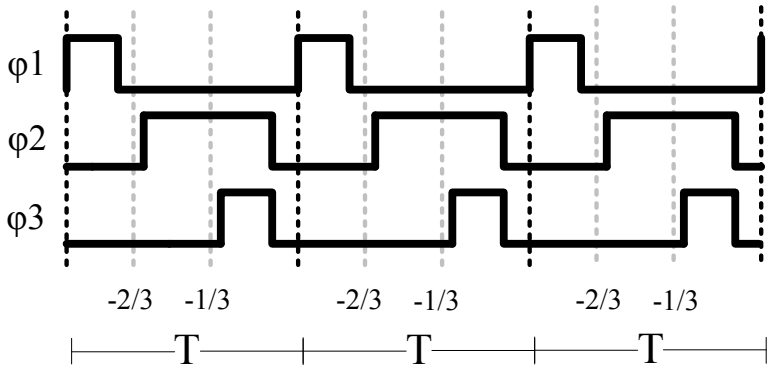
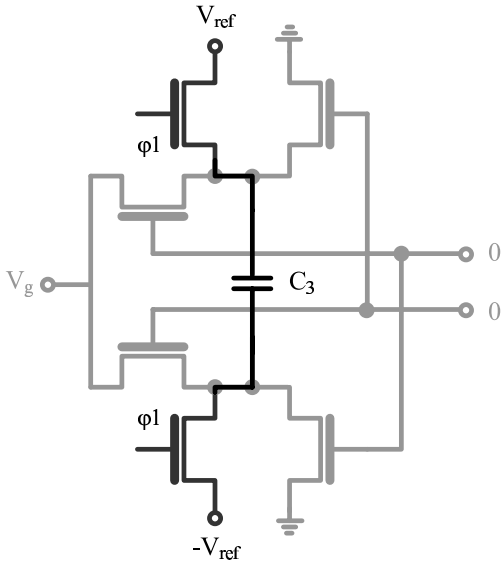
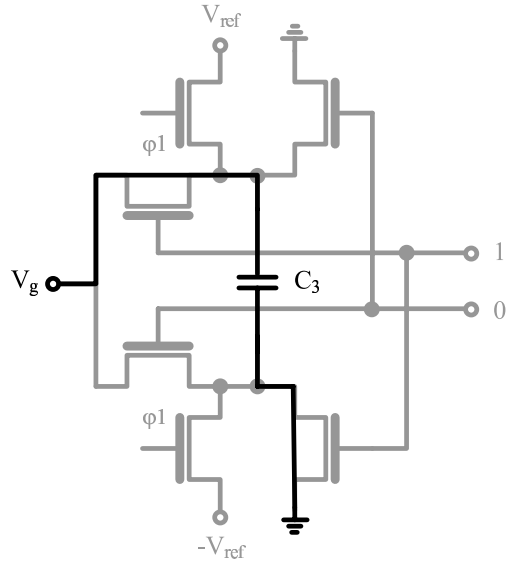


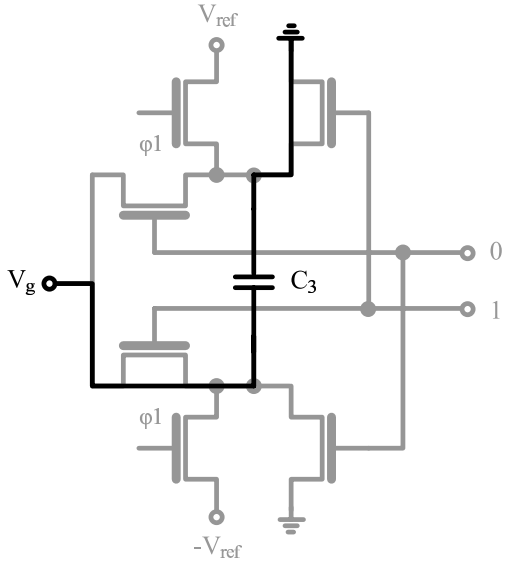
Figure 5.11: Timing diagram for the modulo integrator



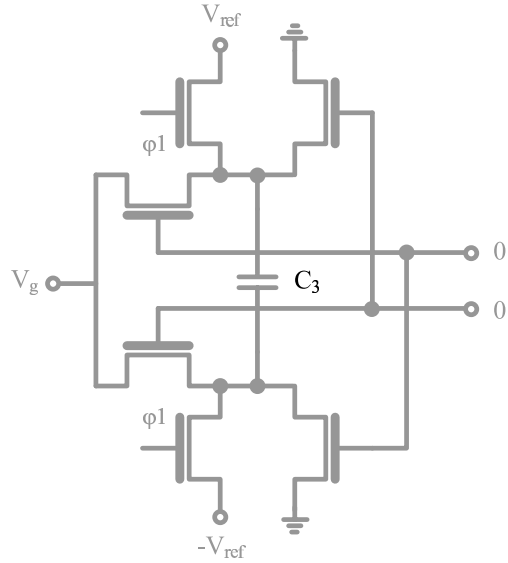
a) In φ1 the capacitor is charged.



b) In φ3, if $V_o \geq V_{ref}$ the charge transfered to V_g will be $Q_3 = C_3V_r$



c) In φ3, if $V_o \leq -V_{ref}$ the charge transfered to V_g will be $Q_3 = -C_3V_r$



d) In φ3, if $-V_{ref} < V_o < V_{ref}$ no charge is transfered to C_3

Figure 5.12: The states of the modulo circuit in Figure 5.10

connections if the output voltage, $V_o(n - T/3)$, is higher than V_{ref}. Here a charge of $Q_3 = C_3V_r$ is transferred to the node V_g in the integrator. This will change the charge transfer equation into

$$C_2V_o(n) = C_2V_o(n - T) + C_1V_i(n - 2T/3) - C_3V_r \tag{5.23}$$

For $V_o(n-T/3)$ lower than $-V_{ref}$, Figure 5.12 c) , the polarity of the charge is reversed and the charge transfer function is

$$C_2V_o(n) = C_2V_o(n - T) + C_1V_i(n - 2T/3) + C_3V_r \tag{5.24}$$

And if $-V_{ref} < V_o(n - T/3) < V_{ref}$ the capacitor C_3 is not connected to V_g and the charge transfer function (5.22) remains unchanged as shown in Figure 5.12 d). Notice that the outputs from the comparators can never be high at the same time.

Combining the three equations, (5.22), (5.23) and (5.24) with $C_1 = C_2 = C_3$ and ignoring the fractional time-steps ($n-T/3$ and $n-2T/3$) the result is (5.5).

The analog modulo integrator presented here resemble a first-order low pass 1.5 bit Sigma-Delta Modulator. If one plots the spectrum of the combined comparator outputs it is a quantized first order noise shaped version of the input. What makes an analog modulo integrator different from a first order low pass Sigma-Delta Modulator is

- The quantizer levels are set at $\pm V_{ref}$, and not evenly distributed between $\pm V_{ref}$.

- The three phase clock implements a form of zero time quantizer feedback, if V_o is higher than V_{ref} V_r is immediately subtracted before the next output of the integrator.

- The comparator outputs are not necessary to reverse the effect of the modulo operation in the digital domain.

5.5 Behavioral Level Verification Of The SC OLSDM

We implemented a macro model description of the SC analog modulo integrator described in the previous section.[3] A single pole operational amplifier macro model with a dc gain of 74dB and a voltage limiter was used to model the operational amplifier. The comparators were modeled as latched comparators. Ideal switches with an on resistance of 200 Ohms were used and the capacitors C1-C3 were 5pF. The reference voltages were $V_{ref} = 1V$ and $-V_{ref} = -1V$. The switch resistance, capacitance and references were chosen arbitrarily. The output of the operational amplifier was limited to $\pm 1.4V$. This ensures that for some values of the input the integrator will saturate during $\phi 2$. The input frequency, sampling frequency and the number of samples was the same as for the Matlab simulation. An overview of the system can be seen in Figure 5.13.

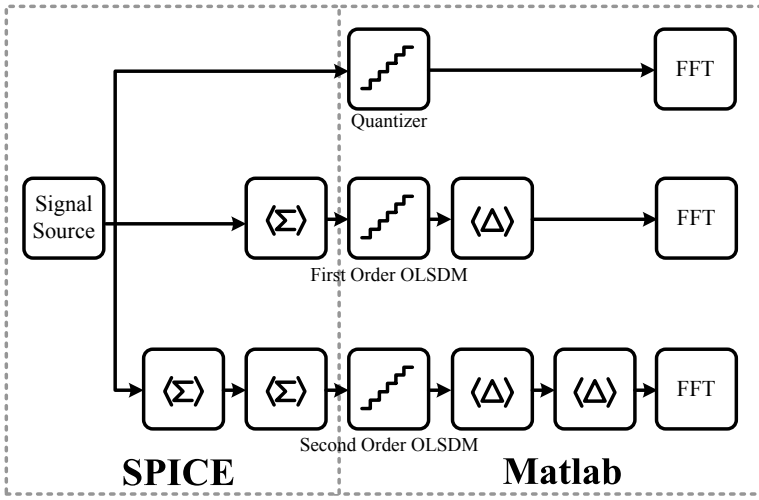


Figure 5.13: Overview of circuit simulation with macro models

Only the analog modulo integrator was implemented in SPICE. Its output was extracted and post-processed in Matlab. The code for the differentiator and the quantizer were the same as in the behavioral simulations.

[3]The SPICE macro model of the switched capacitor analog modulo integrator can be downloaded from http://www.nextgenlab.net/olsdm

In Figure 5.14 the input signal (dark gray) and the output signal (light gray) of the first order SC modulo integrator is shown for the first 150 samples. The sinusoidal input had an amplitude of $0.9V$. The output, V_o, has been sampled at the end of $\phi 3$ and it can be seen how it never exceeds the references at V_{ref} and $-V_{ref}$.

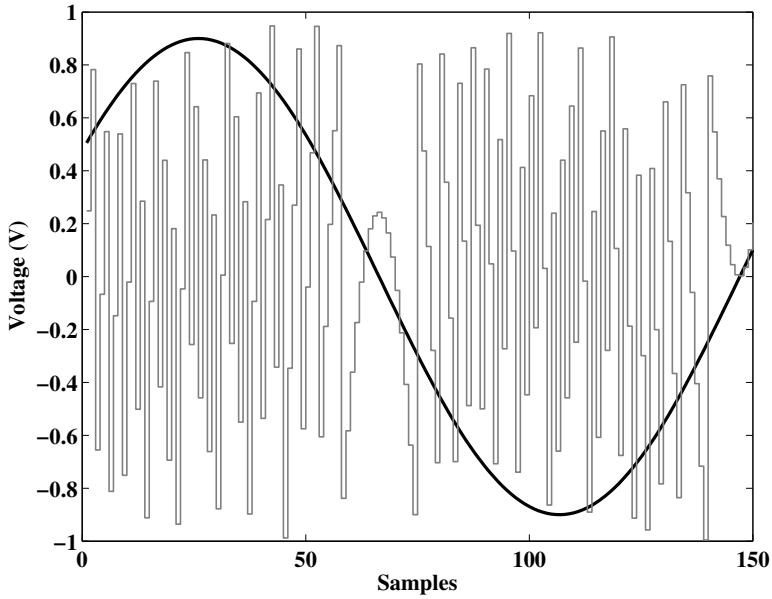


Figure 5.14: Input vs output for the modulo integrator. Input is a sine with an amplitude of 0.9 V

A transient simulation was performed. The results are summarized in Table 5.3. If we remove the effect of reduced input signal amplitude the errors are $-0.2dB$ for first order OLSDM and $-2.1dB$ for second order OLSDM. The error for first order OLSDM is within the error of the SNDR extraction. The error for the second order OLSDM it is to large to be caused by deviations due to SNDR extraction. This extra loss of $-2.1dB$ was mainly due to non-linearity of the voltage limiter used in the simulation. When the voltage limiter is removed the error for second order OLSDM is reduced to $-0.79dB$. The remaining difference is mostly due to finite gain in the operational amplifier. The FFTs of the first and second order OLSDM are shown in Figure 5.15 and Figure 5.16, the ideal quantizer in light gray

and the OLSDM output in dark gray.

Table 5.3: SNDR of OLSDM modulators in SPICE

Noise Shaping	Total (dB)	Difference from Ideal (dB)
First order	64.7	-1.1
Second order	73.1	-3

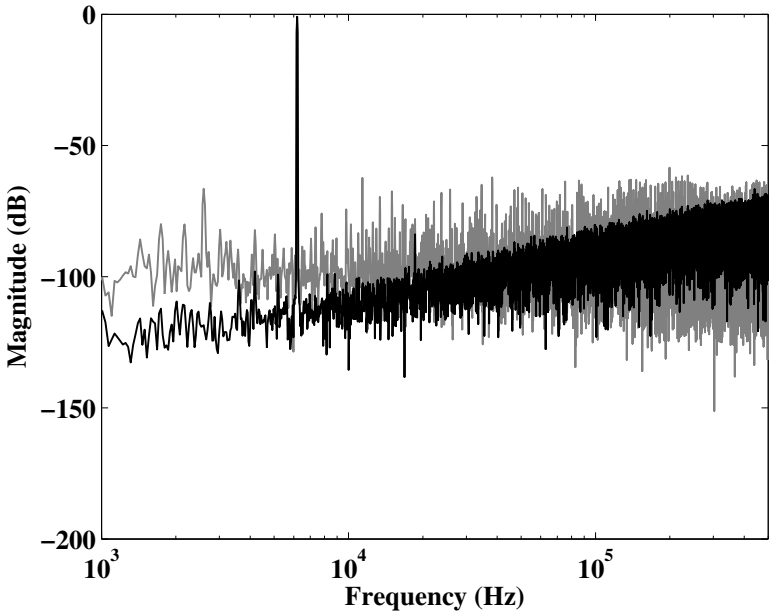


Figure 5.15: FFT of output from first order OLSDM simulation in SPICE.

5.6 Future Work

There are no integrated circuit implementations of an amplitude modulated OLSDM as of yet. An integrated circuit implementation would be the next step. It is needed to check whether the amplitude modulated OLSDM has a place in the family of analog-to-digital converters, or whether it is just of academic interest. There are many questions to be answered and some questions that have not yet been asked. The switched capacitor analog modulo integrator is, to our knowledge, new circuit, and it may find applications

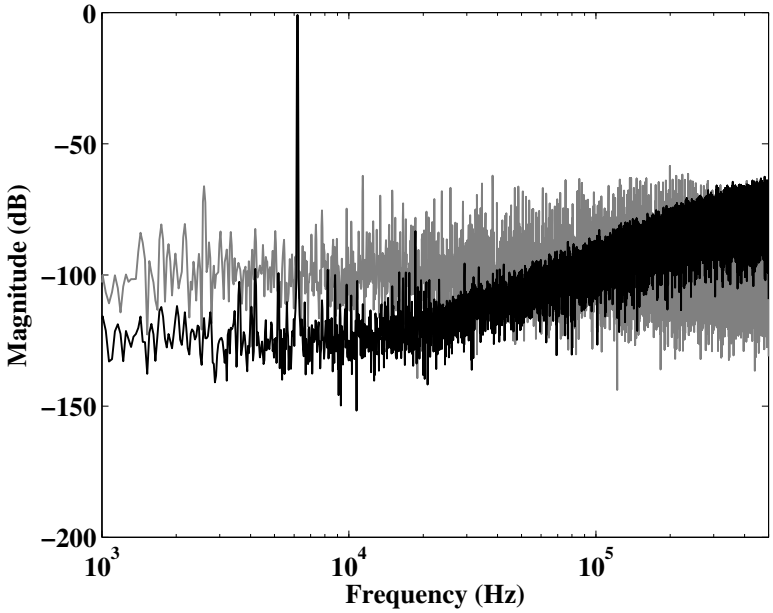


Figure 5.16: FFT of output from second order OLSDM simulation in SPICE.

outside the realm of OLSDM.

5.7 Conclusion

We introduced the switched capacitor analog modulo integrator, which to our knowledge is a new circuit. We introduced the amplitude modulated open loop Sigma-Delta modulator (OLSDM), which is an analog modulo integrator followed by a quantizer and a modulo differentiator. The mathematical equivalence between low pass Sigma-Delta modulators and OLSDM was explained. Behavioral simulations confirmed the equivalence. The necessary circuit, a switched capacitor analog modulo integrator, was explained in detail. Behavioral level simulations in SPICE of the analog modulo integrator verified the function, and proved the concept of amplitude modulated OLSDM.

Acknowledgments

Financial support from the Norwegian Research Council through the project Smart Microsystems for Diagnostic Imaging in Medicine (project number 159559/130) and the project ASICs for Microsystems (project number 133952/420) is gratefully acknowledged.

Chapter 6

Paper 3

Resonators In Open-Loop Sigma-Delta Modulators

Carsten Wulff and Trond Ytterdal

Submitted to IEEE Transactions on Circuits and Systems I: Regular papers

Errata

We recieved a response to this paper quite quickly, and all reviewers found the paper interesting, but wanted more information. We were asked to submit a new version for review with the following changes.

- Discuss the effects of mismatch in capacitors
- Discuss why adding zeros at non-zero frequency is better than at zero frequency
- Add more introduction to OLSDM and SDM
- Discuss the effects of offset errors in comparators

These changes have been included in the paper below.

Abstract

In this paper we introduce the modulo resonator for use in *open-loop sigma-delta modulators* (OLSDM). The OLSDM presented in this work is intended for use in high accuracy (14-bit), high-speed analog-to-digital converters.

The modulo resonator is used with a modulo notch filter to insert a zero in the noise transfer function at a non-zero frequency. The effect of finite gain in modulo integrators and modulo resonators are described and verified through simulation. The modulo resonator and previously published modulo integrator are used in a behavioral model of a switched-capacitor fifth-order OLSDM with more than 13-bit effective number of bits for an oversampling ratio of four. We prove for the N-order OLSDM that the number of bits in the quantizer (B) must be larger than N to ensure equivalence between OLSDM and sigma-delta modulation.

Keywords Sigma-delta modulators, switched-capacitor circuits, modulo integrator, modulo resonator, open-loop sigma-delta modulators

6.1 Introduction

If one wants to make an analog-to-digital converter with high resolution (>12-bit) a sigma-delta modulator is a natural choice. Sigma-delta modulators are prevalent as analog-to-digital converters in applications with low to medium bandwidth (< 10MS/s) and high resolution. The sigma-delta modulator trades speed for resolution. It typically uses a low-resolution quantizer (< 6-bit) with a large quantization error. The quantizer is run at a higher speed than required by the system bandwidth. By using clever analog-filters and feedback techniques the in-band quantization error can be lowered, while the out-of-band quantization error can be large. This out-of-band quantization error is easily filtered using digital filters.

The family of sigma-delta modulators is large, with many diverse family members. One of the oldest members is the low-pass sigma-delta modulator, which in its simplest form consists of an integrator followed by a quantizer. The quantized signal is fed-back to the input through a digital-to-analog

converter (DAC) and subtracted from the input. The transfer function of the modulator is different for the input signal and the quantization noise.[1] The input signal will undergo an integration followed by a differentiation and have a transfer function of one. The quantization noise will be differentiated and thus high pass filtered.

In an ideal world, with no voltage swing limitations, a low-pass sigma-delta modulator could be implemented by an integrator followed by a quantizer and a differentiator, but since supply voltage is limited in electronic circuits, and an integrator has infinite DC gain, it is difficult to implement. Somehow the output swing of the integrator has to be limited. Feedback is typically used to limit the output swing of the integrator.

In this paper we discuss a small sub group that we denote Open-loop sigma-delta modulators (OLSDM). We define OLSDM as *any sigma-delta modulator that does not have feedback of the quantized modulator output signal.*

The idea of a open-loop sigma-delta modulator is to use a limiting function (for example a modulo) to limit the signal swing in the analog domain, replacing the feedback of the quantized signal. After quantization the inverse limiting function is used to reverse the effects of the limit in the analog domain. This idea is by no means new. One of the first suggestion of an OLSDM was almost thirty years ago in [11]. Although there was no system implementation they explained a method that avoided feedback of the quantized signal. Little over a decade ago the Frequency Sigma-Delta Modulator (FSDM) [19] was presented, and more recently [20]. In the FSDM a voltage controlled oscillator (VCO) is used as the modulo integrator, and it was shown in [19] that the pre-processing in FSDM is equivalent to modulo integration. The non-feedback Sigma-Delta digital-to-analog modulator, where the integrator is implemented as a digital modulo integrator, was described in [8]. In [21] an amplitude modulated switched-capacitor open-loop sigma-delta modulator was introduced. A switched-capacitor modulo integrator was used to perform the modulo integration.

[1] This assumes a linear model of the quantizer, since the transfer function is only defined for a linear system

An example of analog-to-digital conversion with open-loop sigma-delta modulation is shown in Fig. 6.1. The input signal, x, is accumulated by the integrator ($\langle\Sigma\rangle$). The integrator in Fig. 6.1 is a modulo integrator that wraps around when the sum exceeds the range (R). The output of the integrator (u) is quantized by a quantizer, which is modeled as a linear addition of quantization noise (q). The conditions for modeling a quantizer as linear addition of noise was covered in [15]. The modulo differentiator ($\langle\Delta\rangle$) reverse the effect of the modulo integrator. The decimation filter required to down-sample the output of the modulator is not shown.

In this modulator the input signal passes through unchanged. The quantization noise pass through the differentiator and is first order high-pass filtered.

The sigma-delta modulator in Fig. 6.1 is equivalent to a first order low-pass sigma-delta modulator providing certain conditions are met.

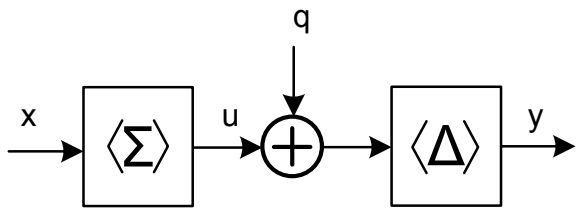


Fig. 6.1: First order low-pass open-loop sigma-delta modulator

The application envisioned for the OLSDM discussed in this paper is as a front-end in a high speed (>10MS/s), high resolution (14-bit) analog-to-digital converter. The advantage of OLSDM is that it is trivial to use high-latency quantizers since there is no feedback of the quantized modulator output.

There are two unsolved challenges that this paper discuss: when is open-loop sigma delta modulation equivalent to sigma-delta modulation, and how to introduce zeros in the noise transfer function (NTF) at non-zero frequencies.

6.1.1 When is OLSDM equivalent to SDM?

It is observed in simulation that open-loop sigma-delta modulation (OLSDM) is not always equal to sigma-delta modulation (SDM). Whether an OLSDM works as an SDM depends on the input signal amplitude and the number of bits in the quantizer. The input signal amplitude must be less than $|x_n| < R/2$ (0dBFS[2]), but OLSDM sometimes loose its noise shaping at less than 0dBFS.

In [21] an error correction scheme was used to restore the noise shaping for input signal amplitudes up to 0dBFS. But the error correction assumed that the input frequency was much less than the sampling frequency ($f_i << f_s$). For some applications (like high speed, high resolution) the OSR can be low ($OSR < 8$) and $f_i << f_s$ is no longer valid.

The number of bits in the quantizer affect the equivalence between OLSDM and SDM. It is observed that the number of bits in the quantizer must be larger than the order of the modulator. This was proved for the special case of a second order OLSDM in [18].

We will prove for the N-order OLSDM that the number of bits in the quantizer (B) must be larger than the order (N) to ensure equivalence between OLSDM and SDM.

6.1.2 Zeros in NTF at non-zero frequency

Previous OLSDMs have all been low order low-pass sigma-delta modulators. Low order low-pass sigma-delta modulators are unsuited for high conversion rate applications due to the high oversampling ratio required to get high resolution, assuming a low resolution quantizer is used.

If the sampling frequency (f_s) is constant, the resolution can be increased by adding more zeros to the noise transfer function (NTF). Adding zeros at a non-zero frequency ($\omega_0 > 0$) reduce the OSR more than adding them at zero frequency. To see why zeros at a non-zero frequency reduce the OSR more than adding them at zero frequency it is instructive to look at a graphical comparison. In Fig. 6.2 a comparison between two fifth-order sigma-delta

[2] 0dB referred to full scale amplitude, $R/2$

modulators is shown, one with all zeros at zero-frequency (dashed line) and one modulator with one zero at zero-frequency and two complex conjugate zeros at non-zero frequencies (solid line). Since the noise transfer function is real the zeros must be complex conjugate, thus to get two zeros at non-zero frequency we need four zeros, two at positive frequencies and two at negative frequencies. The dominating contribution from the noise transfer functions will be at high frequencies. So although the NTF with non-zero frequency zeros has less attenuation at low frequencies it has more attenuation at high frequencies (for example at a normalized frequency of 0.1 the difference is almost 20dB). Accordingly, for an oversampling ratio of four (marked by the dotted line), the NTF with zeros at a non-zero frequency has more attenuation, and as a consequence yields a higher resolution for a given OSR.

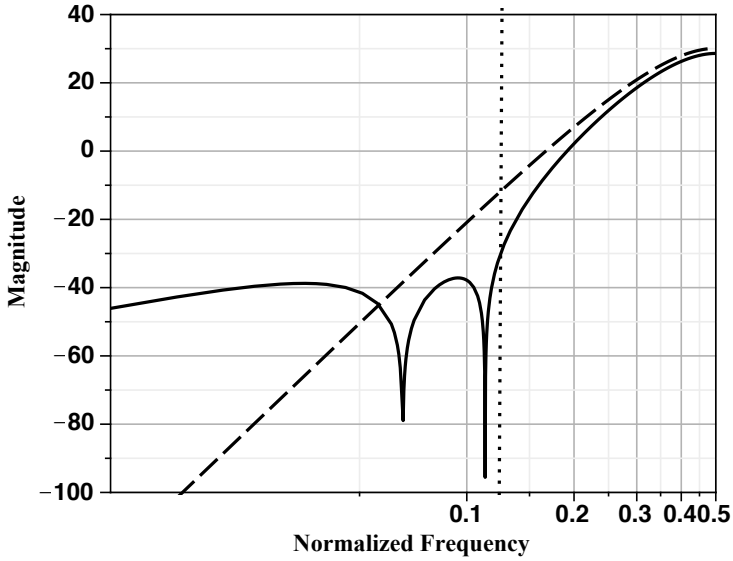


Fig. 6.2: Comparison between a fifth-order sigma-delta modulator with all zeros at zero frequency (dashed-line) and fifth-order sigma-delta modulator with one zero at zero frequency and two complex conjugate zeros at optimum frequencies.

To the best of our knowledge, zeros at non-zero frequencies have not been used in OLSDM before this work.

The paper is organized as follows: In Section 6.2 OLSDM is explained and requirements for input signal amplitude and quantizer bits are derived. In Section 6.3 the key component of OLSDM, the modulo integrator, is described in detail, including the effects of finite gain in modulo integrators. The modulo integrator has previously been described in [21], but the effects of finite gain in modulo integrators has not been exhaustively covered.

The modulo resonator is introduced in Section 6.4. The modulo integrator and modulo resonator are combined in Section 6.5 to make a behavioral model of a fifth order low-pass OLSDM with more than 13-bit effective number of bits with an OSR of four. Simulation results from behavioral level models in MATLAB [22] and SPICE are presented in Section 6.5.

6.2 When is OLSDM equivalent to SDM?

The modulo operator is used extensively in OLSDM to limit the signal swing at the output of modulo integrator. The modulo operator is written as

$$x_r = \langle x \rangle_R \tag{6.1}$$

where $x \in \langle -\infty, \infty \rangle$ is the input signal, R is the range and $x_r \in \langle -R/2, R/2 \rangle$ is the residue after dividing by the range, R. This modulo function is not the normal mathematical modulo function, but a function that computes the remainder of the input signal after rounding it to an integer number of full scale signal swings (R).

The modulo is similar to what was used in [23] where they proved the equivalence of the open-loop and closed loop representations by symbolic manipulation. The modulo arithmetic used in OLSDM has previously been used in comb filters, as was shown in [24].

The following theorem is useful for the derivations below.

Theorem 1 *The modulo of the sum of modulo is equal to the modulo of sum if the range of the two modulus are equal,* $R_0 = R_1 = R$

$$\langle \langle x \rangle_{R_0} + \langle y \rangle_{R_0} \rangle_{R_1} = \langle x + y \rangle_R \tag{6.2}$$

A proof of the theorem is included in Section 6.7

The modulo integration, shown in Fig 6.1, is written as

$$u_n = \left\langle \sum_{i=0}^{\infty} x_{n-i-1} \right\rangle_R \tag{6.3}$$

where x_n is the input signal to the integrator at time n, u_n is the modulator output signal, and n is the discrete time step. The input signal at time $n-1$ is written as x_{n-1}.

The output of the modulator in Fig. 6.1 is

$$y_n = \langle u_n - u_{n-1} + q_n - q_{n-1} \rangle_R \tag{6.4}$$

where q_n is the quantization noise.

Insert (6.3) in (6.4) and let $e_n = q_n - q_{n-1}$

$$y_n = \left\langle \left\langle \sum_{i=0}^{\infty} x_{n-i-1} \right\rangle_R - \left\langle \sum_{i=0}^{\infty} x_{n-i-2} \right\rangle_R + e_n \right\rangle_R \tag{6.5}$$

With (6.2) (6.5) reduces to

$$y_n = \langle x_{n-1} + e_n \rangle_R \tag{6.6}$$

The discrete time equation for a first order low-pass sigma-delta modulator is

$$y_n = x_{n-1} + q_n - q_{n-1} \tag{6.7}$$

Equation (6.6) is equal to (6.7) if

$$|x_n + e_n| < R/2 \tag{6.8}$$

The absolute value of the filtered quantization noise ($|e_n|$) has a maximum value of one LSB (Least Significant Bit), since $|q_n| \leq 1/2LSB$ and $e_n = q_n - q_{n-1}$. Here $LSB = R/2^B$, where B is the number of bits in the quantizer.

The input signal for first order open-loop sigma-delta modulator must

be limited by

$$|x_n| < R/2 - 1LSB = R(1/2 - 1/2^B) \tag{6.9}$$

We will derive the general input signal limitations for N-order OLSDM, but to reduce the length of equations we define

$$f_{x,n} = \sum_{i=0}^{\infty} x_{n-i} \tag{6.10}$$

and from (6.2)

$$\langle \langle f_{x,n} \rangle_R - \langle f_{x,n-1} \rangle_R + e_n \rangle_R = \langle x_n + e_n \rangle_R \tag{6.11}$$

For second order OLSDM (Fig. 6.3) the output of the first integrator is

$$u_n = \langle f_{x,n-1} \rangle_R \tag{6.12}$$

and the output of the second integrator is

$$u_{1,n} = \langle f_{u,n-1} \rangle_R \tag{6.13}$$

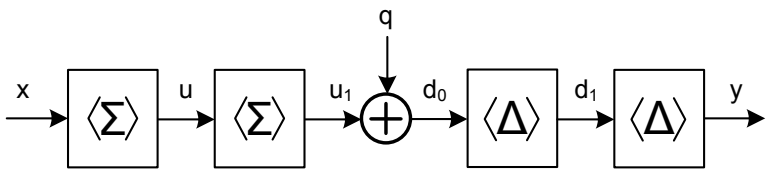


Fig. 6.3: Second order low-pass open-loop sigma-delta modulator

The quantized signal is

$$d_{0,n} = \langle f_{u,n-1} \rangle_R + q_n \tag{6.14}$$

And the output signal of the first modulo differentiator is

$$d_{1,n} = \langle \langle f_{u,n-1} \rangle_R - \langle f_{u,n-2} \rangle_R + e_n \rangle_R \tag{6.15}$$

which by (6.11) is written as

$$d_{1,n} = \langle u_{n-1} + e_n \rangle_R \tag{6.16}$$

The output signal of the modulator is

$$y_n = \langle \langle f_{x,n-1} \rangle_R - \langle f_{x,n-2} \rangle_R + e_n - e_{n-1} \rangle_R \tag{6.17}$$

which by (6.11) is

$$y_n = \langle x_{n-1} + q_n - 2q_{n-1} + q_{n-2} \rangle_R \tag{6.18}$$

The maximum absolute value of the quantization noise in (6.18) is

$$|q_n| + |2q_{n-1}| + |q_{n-2}| = 1/2 + 1 + 1/2 = 2 \tag{6.19}$$

From this it follows that the input signal must be limited by

$$|x_n| < R/2 - 2LSB = R(1/2 - 2/2^B) \tag{6.20}$$

(6.20) is sufficient to ensure that the second order OLSDM is equivalent to a second order SDM. It can be shown that for third order OLSDM the requirement is

$$|x_n| < R/2 - 4LSB = R(1/2 - 4/2^B) \tag{6.21}$$

For N-order OLSDM the input signal must be limited by

$$|x_n| < R(1/2 - 2^{N-1}/2^B) \tag{6.22}$$

If $B = N$ the input signal limit is not practical since

$$|x_n| < R(1/2 - 2^{N-1}/2^B) = R(1/2 - 1/2) = 0 \tag{6.23}$$

Accordingly, $B > N$ to ensure that N-order OLSDM is equivalent to N-order SDM. This is equivalent to the quantizer non-overload criteria in SDM

proved in [25]. An N-order sigma-delta modulator will not overload the quantizer if the input signal is limited by $|x_n| < R/4$, and $B = N + 1$.

For $B = N + 1$ in (6.22)

$$|x_n| < R(1/2 - 1/4) = R/4 \tag{6.24}$$

In the next section we will cover the key component of analog-to-digital OLSDM, the modulo integrator.

6.3 Modulo integrator

In this section we discuss the implementation of a modulo integrator in behavioral level models, the switched-capacitor implementation, and effects of finite opamp gain in the modulo integrator.

6.3.1 Behavior level implementation

The output of the modulo integrator is described by

$$u_n = \left\langle \sum_{i=0}^{\infty} x_{n-i-1} \right\rangle_R \tag{6.25}$$

In behavioral level models (6.25) is impractical due to the infinite modulo. In the definition of the modulo (6.1) the input signal can take any value, $x_n \in \langle -\infty, \infty \rangle$. This requires the modulo integrator to wrap around infinitely many times if the output signal is to be limited by $u_n \in \langle -R/2, R/2 \rangle$. But since the input signal is limited by (6.22), the infinite modulo is unnecessary. Assume that $|x_n| < R/2$, which by (6.22) must be true, then the maximum value after integration ,but before the modulo, is limited by $u_{before,n} \in \langle -R, R \rangle$. Fig. 6.4 shows an example of the output ($u_{before,n}$) before modulo, and after modulo (u_n) for a sinusoidal input signal (x_n). The modulo integrator is implemented by adding or subtracting the range R. The modulo operation can now be defined as

$$u_{before,n} = u_{n-1} + x_{n-1} \tag{6.26}$$

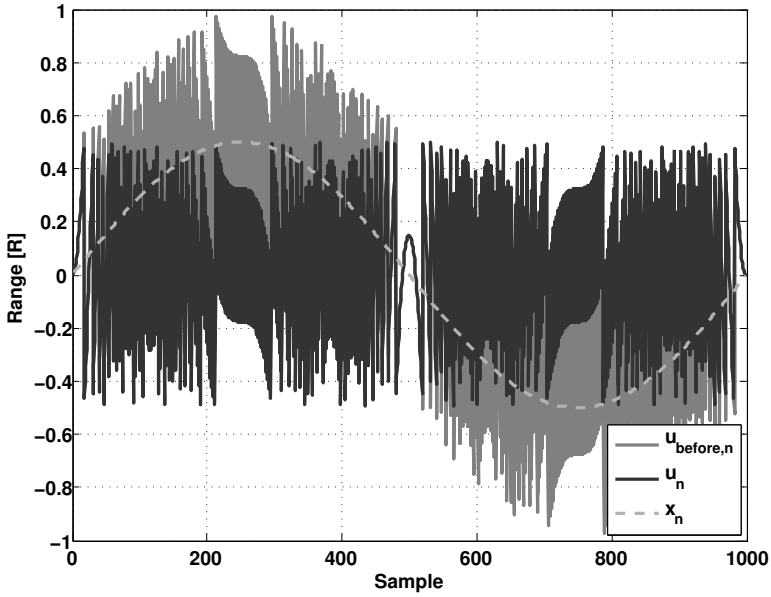


Fig. 6.4: States of the modulo integrator for a sinusoidal input x_n. The output before modulo is $u_{before,n}$ and the output after is u_n.

and

$$u_n = \begin{cases} u_{before,n} + R & u_{before,n} \in \langle -R, -R/2] \\ u_{before,n} & u_{before,n} \in \langle -R/2, R/2\rangle \\ u_{before,n} - R & u_{before,n} \in [R/2, R\rangle \end{cases} \tag{6.27}$$

The modulo integrator described by (6.27) can be implemented as a switched-capacitor (SC) circuit [21].

6.3.2 Switched-capacitor modulo integrator

The SC modulo integrator is based on the parasitic insensitive integrator shown in Fig. 6.5. The input signal is sampled at the end of p_1. In p_2 the charge of C_1 is moved to C_2 by forcing node V_x equal to zero with the opamp. The switched-capacitor modulo integrator is shown in Fig. 6.6. Three clock phases are needed for the modulo integrator, p_1, p_2, and p_3. The clock period is divided into four equally large phases t_0, t_1, t_2, t_3 for a

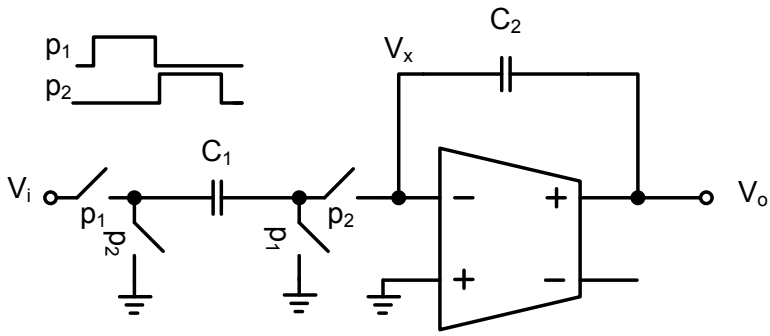


Fig. 6.5: Parasitic insensitive switched-capacitor integrator

straightforward implementation. Phase one is the combination of the first two phases ($p_1 = t_0 + t_1$), phase two is the combination of the last two phases ($p_2 = t_2 + t_3$), and phase three is equal to the last phase ($p_3 = t_3$).

The input signal V_i is sampled across capacitor C_1 during p_1. In p_2 the charge across C_1 is moved to C_2. In p_3 the two comparators in Fig. 6.6 determine whether the output V_o exceeds the references (V_{REF} and $-V_{REF}$), here $|V_{REF}| = R/2$. Capacitor C_3 has been pre-charged in p_1 to $V_{REF} - -V_{REF} = R$.

If the output voltage is larger than V_{REF} C_3 is connected to V_x such that a charge equal to R is subtracted from C_2. If the output voltage is less than $-V_{REF}$ a charge equal to R is added to the charge of C_2. The charge transfer equations for Fig. 6.6 are (6.28) if $V_{o,p_2} \in \langle -V_{REF}, V_{REF} \rangle$, (6.29) if $V_{o,p_2} \in \langle -V_R, V_{REF}]$ and (6.30) if $V_{o,p_2} \in [V_{REF}, V_R \rangle$.

$$C_2 V_{o,n} = C_2 V_{o,n-1} + C_1 V_{i,n-1} \tag{6.28}$$

$$C_2 V_{o,n} = C_2 V_{o,n-1} + C_1 V_{i,n-1} + C_3 V_R \tag{6.29}$$

$$C_2 V_{o,n} = C_2 V_{o,n-1} + C_1 V_{i,n-1} - C_3 V_R \tag{6.30}$$

If $C_1 = C_2 = C_3$ the charge transfer equations implement the modulo defined in (6.27). The modulo operation ensures that the output signal in

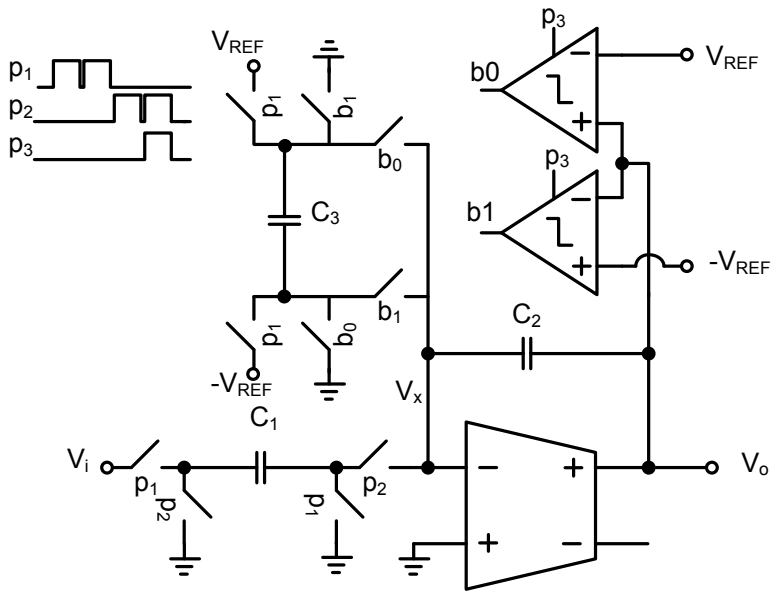


Fig. 6.6: Switched-capacitor modulo integrator

p_3 stays within $V_o \in \langle -V_R/2, V_R/2 \rangle$ as long as $V_i \in \langle -V_R/2, V_R/2 \rangle$.

6.3.3 Effects of finite gain in modulo integrators

One of the non-idealities in SC integrators is the finite opamp gain. The effects of finite opamp gain was covered in [26] and [27]. The transfer function of an integrator with finite gain can be approximated by

$$\frac{V_o(z)}{V_i(z)} = \frac{C_1}{C_2} \frac{az^{-1}}{1 - bz^{-1}} \tag{6.31}$$

where

$$a = 1 - \frac{1 + C_1/C_2}{A_0} \tag{6.32}$$

$$b = 1 - \frac{1}{A_0} \tag{6.33}$$

and A_0 is the DC gain of the opamp. The derivation of this is included in Section 6.8. A block model of the modulo integrator is shown in Fig. 6.7.

We have assumed that the modulo operation does not influence the

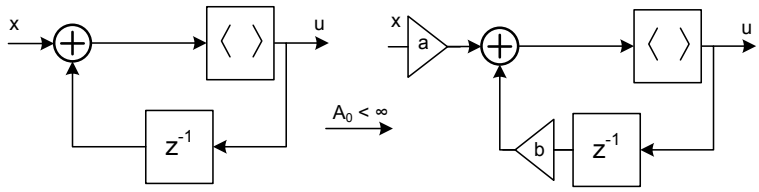


Fig. 6.7: Block model of the modulo integrator for finite DC gain.

effects of finite gain. To verify the model in Fig. 6.7 it is implemented in Simulink [28] and compared with two other models, one based on the difference equations and one based on a SPICE implementation.

An expression can be derived for the output of a first-order OLSDM using the modulo arithmetic used in Section 6.2. The output of a first order OLSDM with finite DC gain in the modulo integrators can be approximated by the difference equation

$$y_n = \left\langle x_{n-1} - \frac{q_{u,n}}{A_0} + q_n - q_{n-1} \right\rangle_R \tag{6.34}$$

where $q_{u,n}$ is a white noise approximation of the modulo integrator output u_n. The derivation is left for Section 6.9.

The difference between (6.34) and (6.6) is the term $-q_{u,n}/A$. Due to the finite opamp gain there is a leakage of u_n to the output. The modulo integrator output (u_n) is a deterministic signal of the input, but we assume it can be approximated as quantization noise with the limits $q_{u,n} \in \langle -R/2, R/2 \rangle$.

From (6.34) the *signal-to-noise and distortion ratio* (SNDR) can be calculated. For a sinusoidal input the SNDR is

$$SNDR = 10 \log \left(\frac{A^2/2}{\frac{1}{12 A_0^2 OSR} + \frac{LSB^2}{12} \times K} \right) \tag{6.35}$$

where A is the amplitude of the sinusoid, the first term in the denominator is the effects of finite gain, and the second term the quantization noise where $K = 2 \int_0^{f_s/2OSR} |NTF(z = e^{j\omega})|^2 df$. The calculation of (6.35) is left for

Section 6.10. With $B = 7$, $OSR = 4$ and $A_0 = 50dB$ the expected SNDR is 51.3dB.

An FFT of the Simulink model (Fig. 6.7) is shown in Fig. 6.8. Fig. 6.9 shows the FFT of the approximate model as defined by (6.34). The FFT of the SPICE model output is shown in Fig. 6.10.

The approximation in Fig. 6.9 is different from the others, here the noise floor is relatively flat up to $0.01f_s$. At that point the shaped quantization noise is larger than the leakage from the integrator output (from (6.34)) and we get the high-pass noise shaping.

For both the Simulink model in Fig. 6.8 and SPICE model in Fig. 6.10 we can see that the contribution $q_{u,n}/A_0$ is not white, but equal to u_n/A_0. Fig. 6.11 shows the FFT of the modulo integrator output (u_n) from the Simulink simulations.

The vertical line in the figures denote the upper bandwidth limit for noise calculation. As a quick estimate of the performance (6.35) works well. It overestimates the effects of noise and has an SNDR of 51.3dB compared to 52.2dB for the Simulink model, 51.66dB in the SPICE model and 51.44dB for the approximation (6.34). These models show that the modulo operation does not significantly influence the equations for the effects of finite gain.

Calculation speed is very different in the three models. Calculating (6.35) takes less than a second, while the Simulink model take ten seconds for 2^{15} points, and the SPICE simulations take a thousand seconds for 2^{15} points.

To increase the resolution of this first order low-pass OLSDM we can either increase the quantizer resolution, which we will not do, or reduce the in-band quantization noise with higher order noise shaping. To get higher order noise shaping we can increase the number of zeros in the noise transfer function (NTF) of the modulator. Either at z=1 (zero frequency) with modulo integrators, or introduce zeros at non-zero frequencies. The next section introduces the modulo resonator, which is used to insert a zero at a non-zero frequency in the noise transfer function.

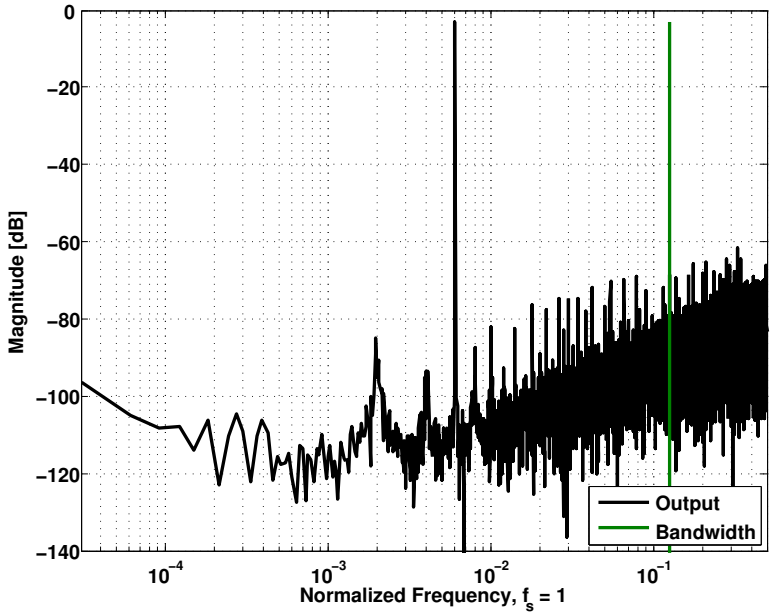


Fig. 6.8: SIMULINK model, SNDR = 52.20-dB

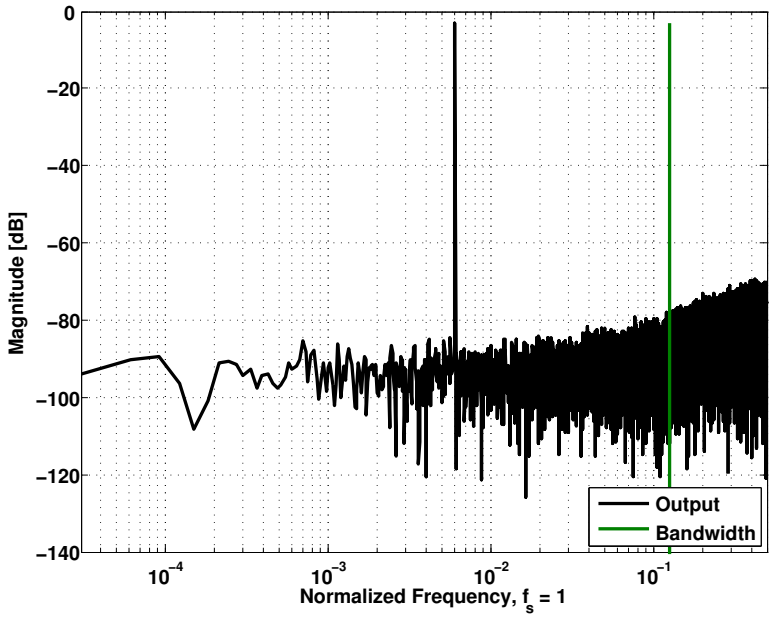


Fig. 6.9: Approximation, SNDR = 51.44-dB

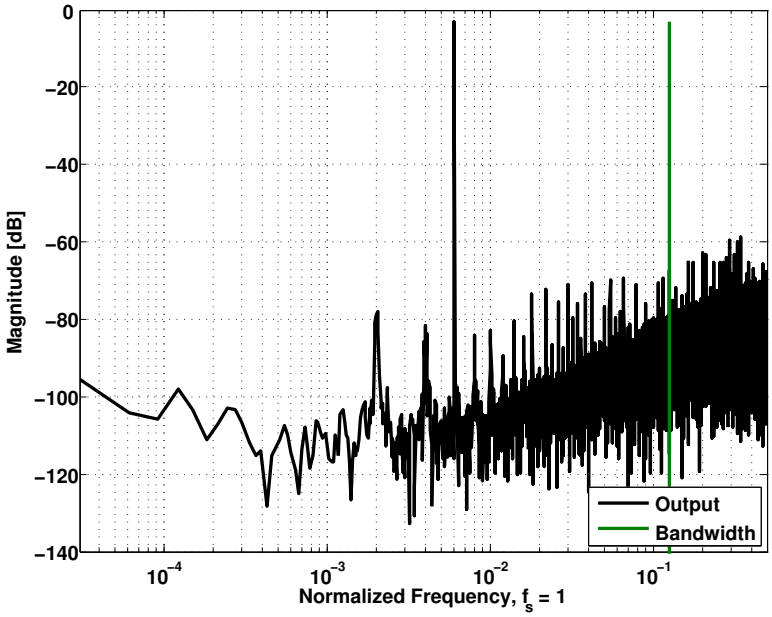


Fig. 6.10: SPICE model, SNDR = 51.66-dB

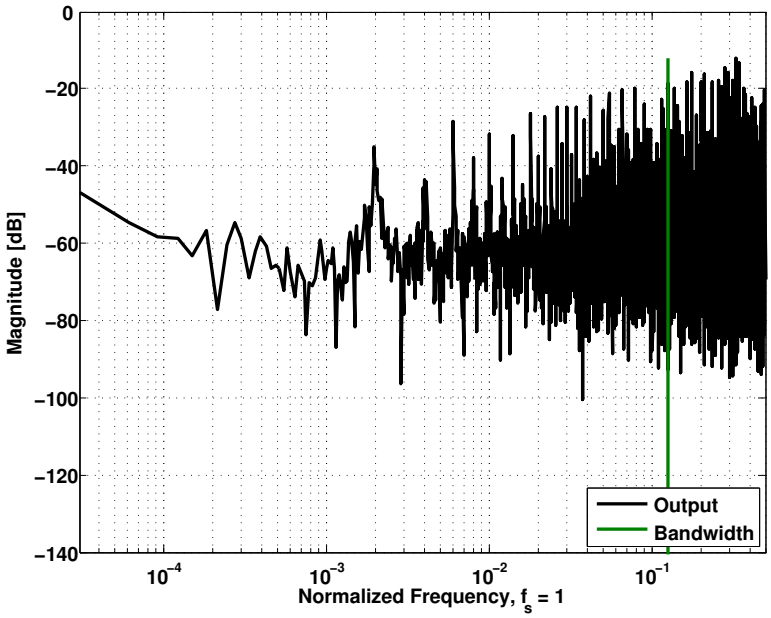


Fig. 6.11: FFT of u_n

6.4 Modulo resonator

Zeros at non-zero frequency in the noise transfer function reduce the oversampling ratio for a given quantizer resolution. With zeros at non-zero frequency one can implement band-pass sigma-delta modulators. In this section the modulo resonator is introduced and the ideal and simulated performance is discussed.

A model of modulator with zeros at non-zero frequency can be seen in Fig. 6.12. In a world without signal swing limitations the input signal (x_n) can be conditioned with a resonator, the output of the resonator quantized, and input signal restored with a notch filter. The quantization noise will pass through the notch filter and be filtered accordingly. The output of the modulator is written as

$$Y(z) = STF(z)X(z) + NTF(z)Q(z) \tag{6.36}$$

$STF(z)$ is the signal transfer function and $NTF(z)$ is the noise transfer function.

The input signal pass through unchanged if the notch filter response matches the resonator response, thus $STF(z) = 1$.[3]

In Fig. 6.12 the $NTF(z)$ is equal to the notch filter response, which has a zero at a non-zero frequency.

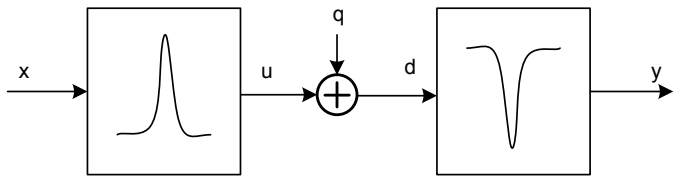


Fig. 6.12: Ideal open-loop implementation of NTF zeros at non-zero frequency

A common resonator used in sigma-delta modulators is based on the lossless discrete integrator (LDI) [29] shown in Fig. 6.13. The LDI resonator

[3]The $STF(z)$ will probably also contain a time delay, depending on the implementation, $STF(z) = z^{-n}$

has a pair of complex conjugate poles at

$$z_p = \rho \pm j\sqrt{(1-\rho^2)}, \rho = 1 - g/2 \tag{6.37}$$

and a resonance frequency of $\omega_0 = cos^{-1}(\rho)$. The advantage of the LDI is the tunable resonance frequency.

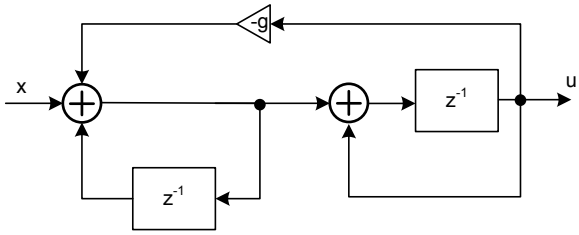


Fig. 6.13: Resonator based on the lossless discrete integrator (LDI)

If the integrators in Fig. 6.13 are replaced with modulo integrators we get the modulo resonator shown in Fig. 6.14. With this modulo resonator we can implement Fig. 6.12 as shown in Fig. 6.15. Fig. 6.15 is a modulo resonator followed by a linear quantizer and a modulo notch filter. The modulo operations at the end of the notch filter reverse the modulo in the resonator. We use two modulo functions in the notch filter since the modulo is defined as (6.27).

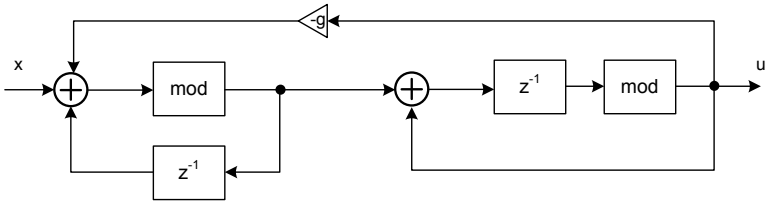


Fig. 6.14: The modulo resonator

The noise transfer function of the modulator in Fig. 6.15 is

$$NTF(z) = z^2 + (g-2)z + 1 \tag{6.38}$$

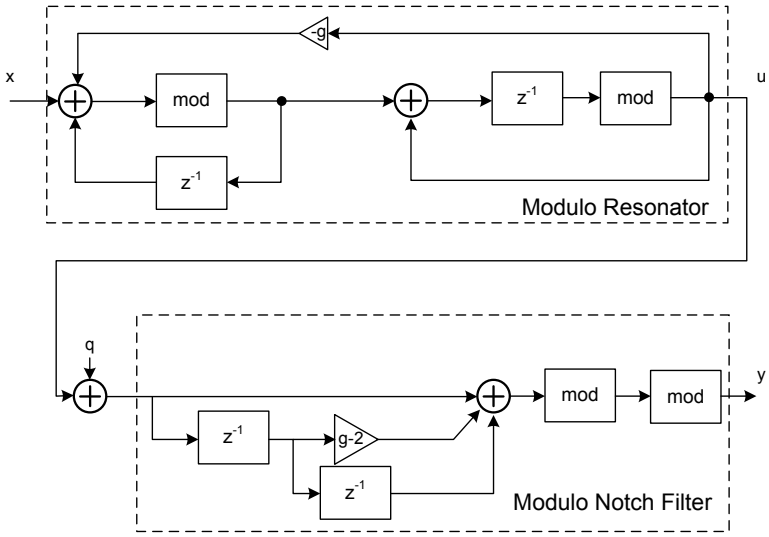


Fig. 6.15: The open-loop sigma-delta modulator with NTF zeros at non-zero frequency

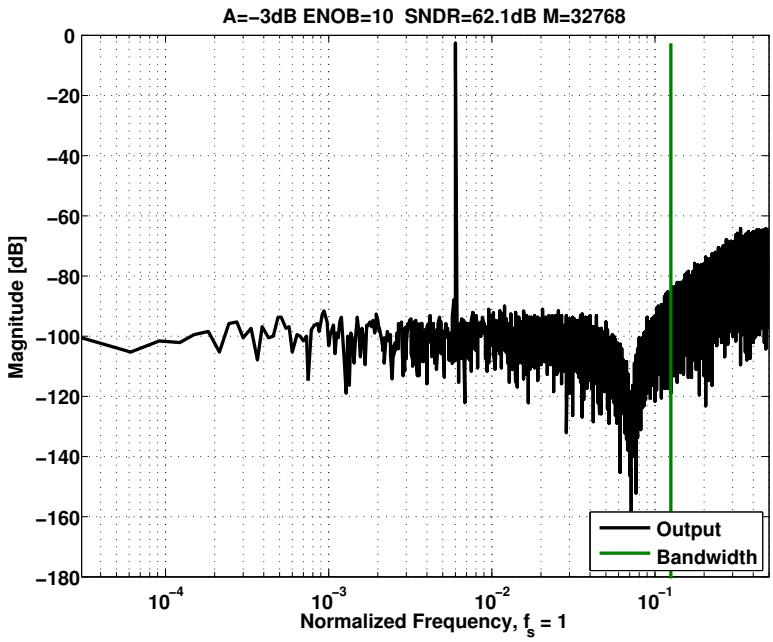


Fig. 6.16: Modulator response. Magnitude of a 2^{15} point FFT. Input signal amplitude is -3dBFS, input signal frequency is at $f_i = 0.006$ with a normalized sampling frequency, $f_s = 1$. The SNDR with $OSR = 4$ is 62.1dB

And has an ideal SNDR of

$$SNDR = 10\log\left(\frac{A^2/2}{2\int_0^{f_s/2OSR} Q_M^2(f)|NTF(z)|^2 df}\right) \tag{6.39}$$

if we assume sinusoidal input. Here $Q_M^2(f)$ is the power spectral density of the quantization noise given by

$$Q_M^2(f) = \frac{LSB^2}{12f_s} = \frac{1}{2^{2B}12f_s} \tag{6.40}$$

where $LSB = R/2^B$ and $R = 1$.

The optimum zero frequency can be calculated from (6.39). Using an OSR of four the optimum zero frequency is $f_i = 0.0718f_s$ ($g = 0.2$). Calculation of the optimum zero frequencies was covered in detail in [30].

Fig. 6.15 was implemented as a Simulink model. Fig. 6.16 is a 2^{15} point FFT of the modulator output (y_n) with an input signal amplitude of -3dBFS and a quantization noise power equivalent to a 7-bit quantizer. Coherent sampling and a Hanning window was used to avoid spectral leakage of the signal power into neighboring FFT bins. A brick-wall filter with bandwidth from $0 - f_s/2OSR$ was used to calculate the SNDR. The vertical line in Fig. 6.16 denotes the bandwidth.

For $f_s = 1$, $OSR = 4$, $B = 7$, $A = 1/\sqrt{8}$ the ideal SNDR from (6.39) is 62dB. The simulated SNDR match the ideal SNDR (1% difference).

6.4.1 Effects of finite gain in modulo resonators

Exact analysis of the effects of finite gain in a modulator with a modulo resonator is complex. The derivation is left for Section 6.11.

The modulator output (y_n in Fig. 6.15) with finite gain in the modulo resonators can be approximated by

$$y_n \approx \langle x_{n-1} + (1+g)\epsilon_{p,n-1} + e_n \rangle_R \tag{6.41}$$

where ϵ_p is the leakage from the first modulo integrator. The shaped quantization noise is represented by e_n. The leakage from the first modulo inte-

grator dominate over the leakage from the second modulo integrator if the opamp gains in the two integrators are equal.

With (6.41) the SNDR is

$$SNDR \approx 10\log\left(\frac{A^2/2}{\frac{(1+g)^2}{12A_0^2}\frac{1}{OSR}+\frac{LSB^2}{12}\times K}\right) \tag{6.42}$$

where $K = \int_0^{f_s/2OSR} |NTF(z)|^2 df$.

Accuracy of (6.42) depend on the DC gain. It overestimates the SNDR with 1.5dB to 1dB for a DC gain of 60dB - 80dB compared to the derivation in Section 6.11. But the leakage from the modulo integrator is approximated by a white noise source, which has higher power than the power of the actual leakage. Accordingly, the two assumptions: leakage approximated by a white noise source, and assuming ϵ_p is the dominating noise source, work in opposite directions.

For A=-3dBFS, $OSR = 4$, $g = 0.2$, $LSB = 1/2^7$ and a DC gain of 60dB, the approximate SNDR from (6.42) is 59.5dB. Whereas for 40dB DC gain the SNDR is 43.1dB.

Using the previously described modulo integrators in a Simulink model of the modulator from Fig. 6.15, the SNDR is 59.2dB for 60dB DC gain and 42.5dB for 40dB DC gain. A difference of 0.3dB (4%) at 60dB DC gain and 0.6dB (7%) at 40dB DC gain.

6.5 Fifth-order low-pass OLSDM

It has previously been shown that the accuracy of SC circuits depend on the capacitor mismatch, finite DC gain and unity-gain bandwidth of the opamp [26], [27]. We have discussed the effects of finite DC gain, but left the derivation of capacitor mismatch and finite unity-gain bandwidth for later work. But we expect the effects to be similar and limit the performance to below 14-bit ENOB. This assumes no calibration or trimming.

Stages in an OLSDM can be pipelined and it is possible to use high

latency quantizers such as pipelined ADCs or SAR ADCs. One in envisioned application of OLSDM is a 14-bit high speed (20MS/s) ADC. In this section we describe a fifth-order OLSDM with an OSR of four and 13-bit ENOB.

6.5.1 Ideal modulator

The modulator is seen in Fig. 6.17. It has two modulo resonators, a modulo integrator, a 7-bit quantizer, a modulo differentiator, and two modulo notch filters. To ensure that (6.22) is satisfied a gain of 0.9 is inserted between the first and second resonators, and between the second resonator and the modulo integrator (this is not shown in Fig. 6.17).

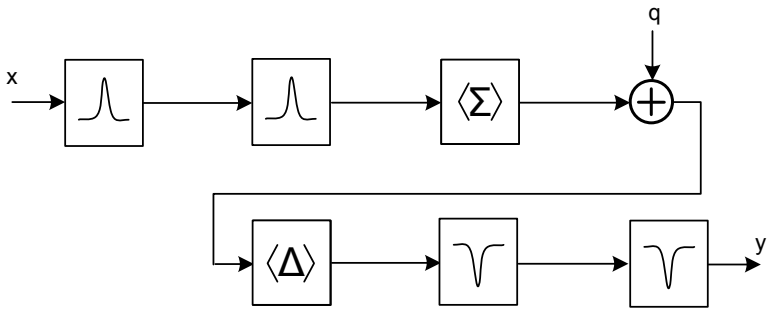


Fig. 6.17: Fifth-order open-loop sigma-delta modulator

The noise transfer function of the modulator in Fig. 6.17 is given by

$$NTF(z) = \frac{(z^2 + (g_1 - 2)z + 1)(z^2 + (g_2 - 2)z + 1)(z - 1)}{0.81} \tag{6.43}$$

And the ideal SNDR can be calculated with (6.39), using the NTF from (6.43). With an OSR of four the optimal constants are $g_1 = 0.17$ and $g_2 = 0.48$. For $OSR = 4$, A=-3dBFS and $B = 7$ the ideal SNDR is 85dB.

A 2^{15} point FFT is calculated from the output of a MATLAB simulation of the ideal modulator in Fig. 6.17. The FFT is shown in Fig. 6.18. The simulated match the ideal SNDR (1% difference).

The input signal must be limited as stated in (6.22). An input signal amplitude of -3dBFS $= 1/\sqrt{8} \approx 0.354$ is used in the simulations. If we

insert for $N = 5$ and $B = 7$ in the input signal limit (6.22)

$$|x(n)| < R(1/2 - 2^{5-1}/2^7) = 0.375 \tag{6.44}$$

Thus the modulator is valid for an input signal amplitude of -3dBFS.

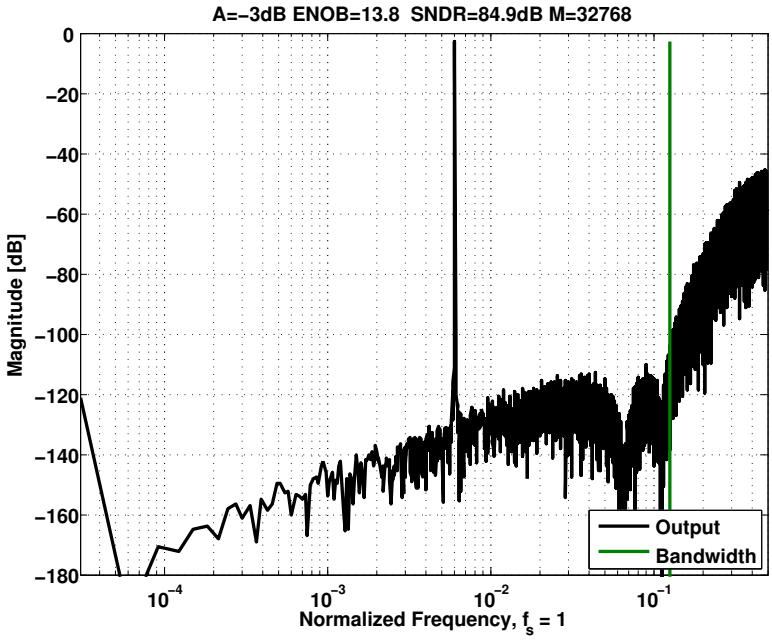


Fig. 6.18: Modulator output. Magnitude of a 2^{15} point FFT of the modulator output. Input signal amplitude -3dBFS. Input frequency $f_i = 0.006$ and sampling frequency $f_s = 1$. With an $OSR = 4$ the SNDR is 84.9dB

6.5.2 Modulator with finite opamp gain in modulo integrators

Fig. 6.19 shows the fifth order sigma-delta modulator with the the modeled opamp gain. The modulo integrators are modeled with an opamp gain of 85dB in the first resonator, 75dB in second resonator, and 65dB in the last modulo integrator. These gains were chosen from design equations based on (6.42). Assume the leakage due to finite opamp gain in the first modulo resonator dominate. The SNDR is then estimated from (6.42). The

estimated SNDR for this modulator is 83.3dB for an input amplitude of -3dBFS. Fig. 6.20 is a 2^{15} point FFT of the modulator output (y_n) using an input signal amplitude of -3dBFS.

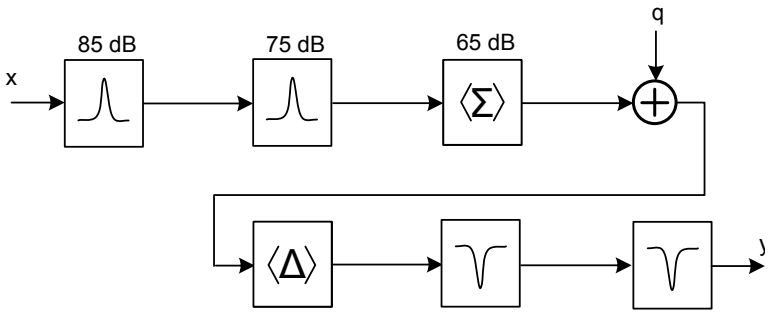


Fig. 6.19: Fifth-order open-loop sigma-delta modulator. The DC gain of opamps are shown above the stages.

The simulated SNDR is 80.9dB (13.15-bit ENOB[4]), or 2.4dB below the estimated SNDR. This is expected due to leakage from later stages. If we increase the DC gain in the second modulo resonator and the last modulo integrator to 200dB, we remove them as noise contributors. This increases the SNDR to 82.8dB, which is 0.5dB (6%) lower than the estimated.

The modulator in Fig. 6.19 was implemented in SPICE as a switched capacitor circuit.

6.5.3 Switched capacitor modulator

Fig. 6.21 shows a switched-capacitor implementation of the modulator. A single ended modulator was used for simplicity.

The opamps have a DC gain of 85dB, 85dB, 75dB, 75dB, and 65dB. The opamp was implemented as a macro-model of a single-pole operational amplifier.

A comparison between the MATLAB model and the SPICE model is shown in Fig. 6.22, here a 2^{15} point FFT was run on both the SPICE and the MATLAB outputs. The SNDR is the same for both models. In SPICE,

[4]ENOB = (SNDR-1.76)/6.02

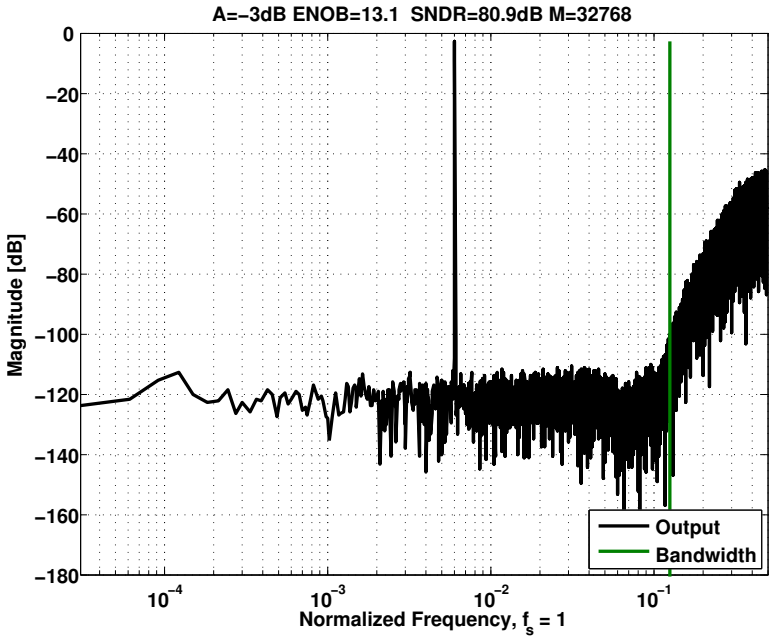


Fig. 6.20: Magnitude of a 2^{15} point FFT of the modulator output. Input signal amplitude -3dBFS, input frequency $f_i = 0.006$ and sampling frequency $f_s = 1$. With an $OSR = 4$ the SNDR=80.9dB

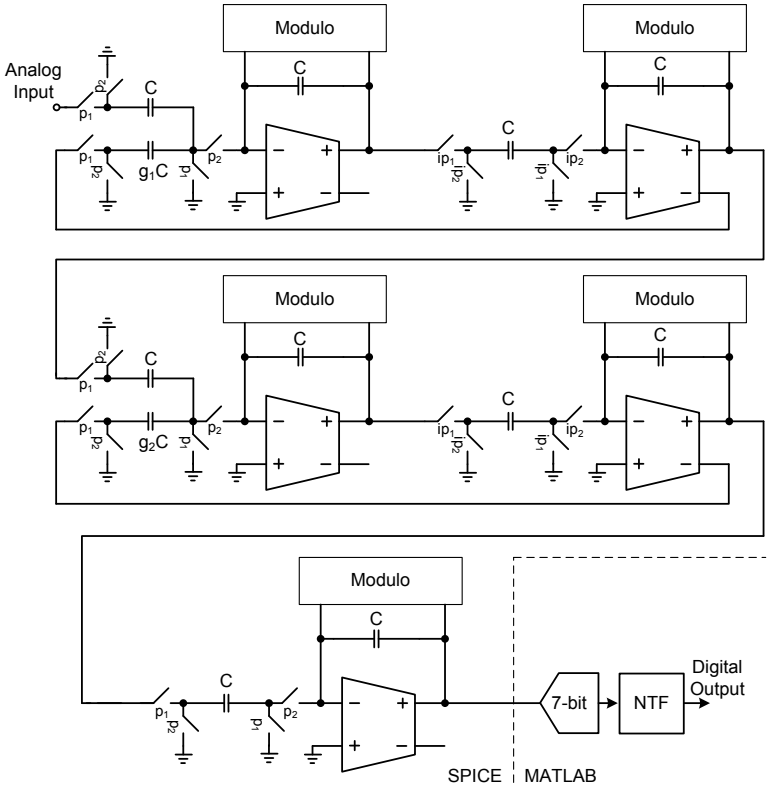


Fig. 6.21: Fifth order OLSDM SPICE model. Quantization and NTF are implemented in MATLAB

however, there is more harmonic content, with the second harmonic visible in the FFT.

The quantizer and NTF for the SPICE simulations is implemented in MATLAB . A 7-bit ideal quantizer is used instead of the linear approximation to quantization noise.

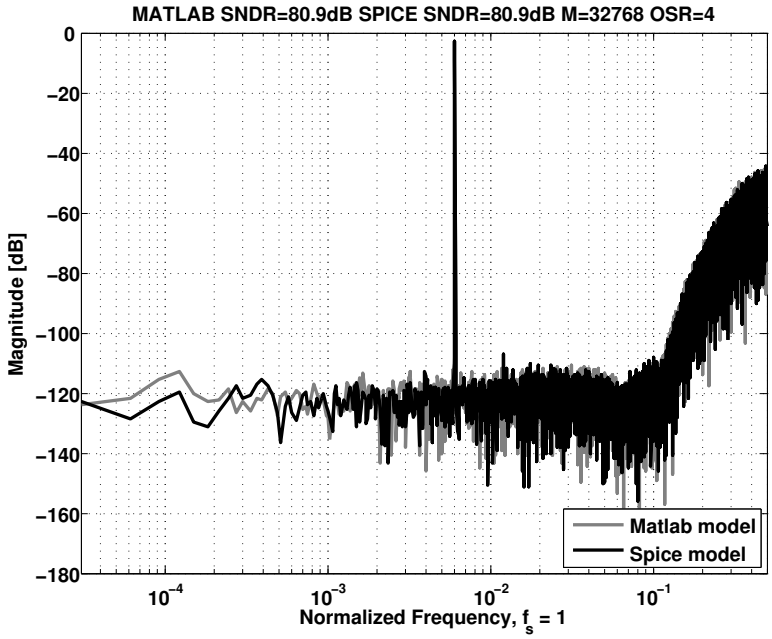


Fig. 6.22: Comparison of SPICE model and MATLAB model. Input signal amplitude -3dBFS, input frequency $f_i = 0.006$ and sampling frequency $f_s = 1$. With an $OSR = 4$ the SNDR is 80.9dB for the MATLAB model and 80.9dB for the SPICE model.

Capacitor mismatch

In modern CMOS processes the matching between capacitors is good. In a typical 90nm process the matching of two 10pF Metal-Insulator-Metal (MIM) capacitors can be as good as 0.06% (3 sigma). In the switched-capacitor OLSDM matching will influence the coefficients, and the inter-stage gain. The matching in the first stage is most critical, as mismatch in later stages is attenuated by the gain of the previous stage. With a mismatch

in the coefficients and inter-stage gain the digital transfer function (from the quantizer and out) will not have the correct coefficients. This will lead to noise leakage, since the poles of the analog filter (the two resonators and the integrator) will not match the zeros in the digital filter (the two notch filters and the differentiator).

With 0.06% matching between capacitors the SNDR degrades to 79.7dB, which is not significant. But the capacitor sizes in a switched-capacitor implementation will be determined by the most critical capacitor, the g_1C capacitor in the first stage. In this example $g_1 = 0.17$, which is small. With mismatch taken into consideration it might be advantageous to move resonator with the $g_2 = 0.48$ first, even though this will increases the noise leakage somewhat. The unit capacitor C can be chosen smaller since the g_2C capacitor must match to 0.06% (3 sigma). With g_1C as the first capacitor the unit capacitor must be almost three times larger than if the g_2C capacitor is used as the first capacitor.

Comparator Offset

A concern with a switched-capacitor implementation is the offset in the comparators used in the modulo resonator. Simulations suggest that the stochastic offset of comparators in the modulo resonator must be within 0.25% of full-scale to have an SNDR of above 77dB. Achieving an offset on this level requires rigorous analog design. At offset of 1% of full-scale the SNDR degrades to 65dB. For example, with a full-scale of 2V peak-to-peak we tolerate an offset of $\pm 5mV$ in the comparator thresholds.

6.6 Conclusion

In this paper we introduced the modulo resonator for open-loop sigma-delta modulators (OLSDM). It was used with a modulo notch filter to introduce a zero in the noise transfer function at a non-zero frequency. The modulo resonator and previously published modulo integrator were used in a behavioral model of a switched-capacitor fifth-order OLSDM with more than 13-bit effective number of bits for an oversampling ratio of four. We proved

that the number of bits in the quantizer (B) must be larger than the order of the modulator (N) to ensure equivalence between OLSDM and sigma-delta modulation.

6.7 Proof of modulo theorem

Proof 1 *From definition*

$$\langle a + nR \rangle_R = \langle a \rangle_R \tag{6.45}$$

where n is an integer. Given

$$\langle \langle x \rangle_R + \langle y \rangle_R \rangle_R \tag{6.46}$$

we can write $\langle x \rangle_R = x - nR$ and $\langle y \rangle_R = y - mR$, where n and m are integers. From (6.45) it follows that

$$\langle x - nR + y - mR \rangle_R = \langle x + y \rangle_R \tag{6.47}$$

6.8 Effects of finite gain in SC integrators

If we assume infinite DC gain in the opamp the charge transfer equation is simply

$$C_2 V_{o,n} = C_2 V_{o,n-1} + C_1 V_{i,n-1} \tag{6.48}$$

The z-domain transfer function of (6.48) is

$$\frac{V_o(z)}{V_i(z)} = \frac{C_1}{C_2} \frac{z^{-1}}{1 - z^{-1}} \tag{6.49}$$

If $C_1 = C_2$, then (6.49) is the well known transfer function of a discrete time integrator and is a good approximation if the DC gain (A_0) is much higher than the accuracy required. If the DC gain is close to, or lower than the accuracy, then (6.49) no longer applies.

With finite opamp gain the voltage V_x (in Fig. 6.5) will be different from zero. A non-zero V_x will result in a residual charge on capacitor C_1

given by $Q_{1,n} = C_1 V_x$. The charge transfer equation change into

$$Q_{2,n} = Q_{2,n-1} + Q_{1,n-1} + Q_{1,n} \tag{6.50}$$

where $Q_2 = C_2(V_o - V_x)$, $Q_{1,n-1} = C_1 V_i$. The residual voltage V_x is equal to $V_x = -V_o/A_0$. We define

$$\alpha = 1 + \frac{1}{A_0} \tag{6.51}$$

If we expand (6.50) we get

$$\alpha V_{o,n} = \alpha V_{o,n-1} + \frac{C_1}{C_2} V_{i,n-1} - \frac{C_1}{C_2} \frac{V_{o,n}}{A_0} \tag{6.52}$$

Solved for V_o/V_i and transferred to the z-domain we get the transfer function

$$\frac{V_o(z)}{V_i(z)} = \frac{C_1}{C_2} \frac{\left(\dfrac{1}{1 + \dfrac{1 + C_1/C_2}{A_0}} \right) z^{-1}}{1 - \alpha \left(\dfrac{1}{1 + \dfrac{1 + C_1/C_2}{A_0}} \right) z^{-1}} \tag{6.53}$$

If we assume $A_0 >> 1$, then (6.53) can be approximated to first order by

$$\frac{V_o(z)}{V_i(z)} = \frac{C_1}{C_2} \frac{\left(1 - \dfrac{1 + C_1/C_2}{A_0} \right) z^{-1}}{1 - \left(1 - \dfrac{1}{A_0} \right) z^{-1}} \tag{6.54}$$

6.9 Effects of finite gain in modulo integrators

From charge transfer equations the output of the modulo integrator is

$$\alpha u_n = \langle \alpha u_{n-1} + x_{n-1} - u_n/A_0 \rangle_R \tag{6.55}$$

where $\alpha = 1 + 1/A_0$ and A_0 is the DC gain of the opamp. We also have

$$\alpha u_{n-1} = \langle \alpha u_{n-2} + x_{n-2} - u_{n-1}/A_0 \rangle_R \tag{6.56}$$

and that

$$\alpha u_{n-2} = \langle \alpha u_{n-3} + x_{n-3} - u_{n-2}/A_0 \rangle_R \tag{6.57}$$

Using (6.2) the output of the modulo integrator is

$$\begin{aligned} u_n &= \frac{\left\langle \sum_{i=0}^{\infty} x_{n-1-i}\alpha^i - \sum_{i=0}^{\infty} \frac{u_{n-i}}{A_0}\alpha^i \right\rangle_R}{\alpha} \\ &= \left\langle \sum_{i=0}^{\infty} x_{n-1-i}\alpha^{i-1} - \sum_{i=0}^{\infty} \frac{u_{n-i}}{A_0}\alpha^{i-1} \right\rangle_R \end{aligned} \tag{6.58}$$

The output of the modulator is

$$y_n = u_n - u_{n-1} + q_n - q_{n-1} \tag{6.59}$$

using (6.2) and (6.58)

$$y_n = \left\langle \frac{x_{n-1}}{\alpha} - \frac{u_n}{A_0\alpha} + q_n - q_{n-1} \right\rangle_R \tag{6.60}$$

Assuming $A_0 >> 1$ we can approximate the modulator output by

$$y_n = \left\langle x_{n-1} - \frac{u_n}{A_0} + q_n - q_{n-1} \right\rangle_R \tag{6.61}$$

The signal u_n can be written as (6.25). This signal is the quantization noise after rounding the integrator output to the range R. We assume this quantization noise is white. Assume $u_n \approx q_{u,n} \in \langle -R/2, R/2 \rangle$. Then (6.61) simplifies to

$$y_n = \left\langle x_{n-1} - \frac{q_{u,n}}{A_0} + q_n - q_{n-1} \right\rangle_R \tag{6.62}$$

6.10 Calculation of the SNDR

The power spectral density of quantization noise is given by the well known equation

$$Q^2(f) = \frac{LSB^2}{12 f_s} \tag{6.63}$$

where f_s is the sampling frequency. For a given bandwidth the noise power is

$$Q^2 = 2\int_0^{f_s/2OSR} Q^2(f)df = \frac{LSB^2}{12}\frac{1}{OSR} \tag{6.64}$$

The LSB of $q_{u,n}/A_0$ can be written as R/A_0. And if we assume $R = 1$ the noise power of the modulo integrator output leakage is given by

$$Q_u^2 = \frac{1}{12 \times A_0^2}\frac{1}{OSR} \tag{6.65}$$

The quantization noise in a first order OLSDM is high-pass filtered, and has a noise transfer function of

$$NTF(z) = 1 - z^{-1} \tag{6.66}$$

The LSB of the quantization noise is $LSB = R/2^B$, so with $R = 1$ the quantization noise power can be calculated from

$$Q_n^2 = 2\int_0^{f_s/2OSR} \frac{1}{12 \times 2^{2B} f_s} |NTF(z = e^{j\omega})|^2 df \tag{6.67}$$

The signal to noise and distortion ratio can be written as

$$SNDR = 10\log\left(\frac{A^2/2}{Q_u^2 + Q_n^2}\right) \tag{6.68}$$

and inserted for (6.65) and (6.67) gives

$$SNDR = 10\log\left(\frac{A^2/2}{\frac{1}{12A_0^2 OSR} + \frac{LSB^2}{12} \times K}\right) \tag{6.69}$$

where

$$K = 2\int_0^{f_s/2OSR} |NTF(z = e^{j\omega})|^2 df \tag{6.70}$$

6.11 Effects of finite gain in modulo resonators

We start with the difference equations for the output of the integrators in the modulo resonator. And we assume that the modulo has no effect. The output of the first modulo integrator is given by

$$\alpha p_n = (1+g)\alpha p_{n-1} + x - g u_n - (1+g)\epsilon_p \tag{6.71}$$

where $\epsilon_p = p_u/A_0 \approx q_p/A_0$ is the leakage as described earlier for modulo integration and $\alpha = 1 + 1/A_0$, where A_0 is the DC gain. The leakage is now $(1+g)$ larger than for a single modulo integrator, which is due to the feedback capacitor given by gC in Fig. 6.21. The feedback capacitor increase the residual charge since the voltage V_x in the modulo integrator is now forced across a larger capacitance $C + gC$. The output of the modulo resonator is written as

$$\alpha u_n = \alpha u_{n-1} + p_{n-1} - \epsilon_u \tag{6.72}$$

where $\epsilon_u = u_n/A_0 \approx q_u/A_0$ is the leakage from the second modulo integrator. Transferring to the z-domain and solving the equations for u we get

$$U(z) = \frac{xz^{-1}}{B(z)} - \frac{(1-z^{-1})\alpha\epsilon_u}{B(z)} - \frac{(1+g)\epsilon_p z^{-1}}{B(z)} \tag{6.73}$$

where $B(z)$ is

$$B(z) = \alpha^2 z^{-2} + (g - 2\alpha^2)z^{-1} + \alpha^2 \tag{6.74}$$

After the modulo resonator the signal is quantized and filtered by the notch filter. The notch filter transfer function is equal to the noise transfer function. The NTF can be written as[5]

$$NTF(z) = z^{-2} + (g-2)z^{-1} + 1 \tag{6.75}$$

[5]Here we have shifted the NTF in time by multiplying by z^{-2}

and we see that if $\alpha = 1$ then $NTF(z) = B(z)$.

The output of the modulator will be

$$Y(z) = U(z) \times NTF(z) + Q(z) \times NTF(z) \tag{6.76}$$

inserted for (6.73) in (6.76)

$$\begin{aligned} Y(z) = \frac{NTF(z)}{B(z)} \left[xz^{-1} + (1 - z^{-1})\alpha\epsilon_u + (1 + g)\epsilon_p z^{-1} \right] \\ + Q(z) \times NTF(z) \end{aligned} \tag{6.77}$$

There are three effects that can be seen from (6.77). The leakage from the first integrator ϵ_p leaks directly to the output scaled by a factor $1 + g$. The leakage from the second integrator, ϵ_u, is first order high pass filtered. The finite gain in the modulo integrators cause an incomplete pole/zero cancellation between the NTF(z) and B(z), for low DC gain this will increase the noise contribution. For high DC gain we can assume that $\alpha \approx 1$ such that $NTF/B(z) \approx 1$. Then (6.77) becomes

$$\begin{aligned} Y(z) = X(z)z^{-1} + (1 - z^{-1})\epsilon_u + (1 + g)\epsilon_p z^{-1} \\ + Q(z) \times NTF(z) \end{aligned} \tag{6.78}$$

Transferred back to time domain we have the difference equation

$$y_n = \langle x_{n-1} + \epsilon_{u,n} - \epsilon_{u,n-1} + (1 + g)\epsilon_{p,n-1} + e_n \rangle_R \tag{6.79}$$

where e_n is the shaped quantization noise.

The dominating noise source in (6.79) is the the leakage from the first integrator ($(1+g)\epsilon_{p,n-1}$). The modulator output can thus be approximated by

$$y_n \approx \langle x_{n-1} + (1 + g)\epsilon_{p,n-1} + e_n \rangle_R \tag{6.80}$$

Chapter 7

Paper 4

0.8V 1GHz Dynamic Comparator In Digital 90nm CMOS Technology

Carsten Wulff and Trond Ytterdal

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21-22 Nov. 2005 Pages 237 - 240
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Errata

- Section 7.2, second paragraph, third sentence: What way → Which way
- Section 7.3, fifth paragraph, second sentence: to threshold → to the threshold

Abstract

The design of a 0.8V 1GHz dynamic comparator in digital 90nm CMOS technology is presented. The work will show that low voltage, low power and high speed analog circuits are feasible in nano-scale CMOS technologies. The dynamic comparator dissipates a maximum of 222μW at 1GHz clock

frequency with 100fF capacitive load and 0.8V supply voltage. This is lower than comparable results.

7.1 Introduction

One of the factors driving the downscaling of CMOS technology is the ever present drive for price-per-performance of digital circuits. The minimum dimensions get smaller and maximum supply voltages are reduced due to reliability issues [31]. Since digital circuits are the driving force of silicon technology, analog circuit designers often have to work in digital CMOS processes. The reduction in supply voltage is not necessarily followed by an equal reduction in threshold voltage, which limits the available voltage headroom [32]. These nano-scale CMOS technologies offer many challenges that have been discussed in previous publications, among others [31–33]. The challenges have, in some cases, brought success to simpler topologies [34] that have shown some of the advantages of nano-scale CMOS for analog circuits. One advantage of scaling down is the increased speed that follows. It can be shown that the unity gain frequency (f_{UG}) of a transistor is proportional to the effective gate voltage (V_{GT}) over the square of the length (L) of a transistor as given by (7.1) [32]

$$f_{UG} \propto \frac{V_{GT}}{L^2} \tag{7.1}$$

Thus the trend will be that shorter lengths bring higher speeds.

Dynamic comparators are a class of circuits often used in pipeline analog to digital converters (ADCs) [35]. As the name suggests a pipeline ADC consists of multiple stages. It is common to extract at least 1.5-bits in each stage. The 1.5-bits per stage stem from a digital error correction algorithm that requires a certain redundancy in the number of bits. With the digital error correction comparators in each stage can have quite large offset. Using 1.5-bits per stage one can tolerate a comparator offset of up to $\pm V_{REF}/4$, where V_{REF} is the high reference voltage minus the common mode voltage. In general, the comparators can tolerate an offset up to $\pm V_{REF}/2^b$ for a

b-bit stage [36]. Using dynamic comparators may reduce the architectural complexity and reduce power dissipation, but tight control over variations and mismatch must be exercised to ensure that offset and other errors are kept within the allowed limits. Architectures that reduce mismatch have been presented [36]. In this paper, we describe a dynamic comparator that is a modification of MOSFET-only fully-differential dynamic comparator presented in [37]. We will first describe the architecture and operation of the comparator before we present the design in 90nm CMOS and simulation results.

7.2 Dynamic comparator architecture

The circuit can be seen in Figure 7.1. In [37] they used a clock booster to supply a higher voltage to M1-M4 than the supply voltage. To avoid any reliability concerns that may come with boosted voltages we have replaced the clock booster with a single transistor M5. The comparator has two phases; Reset and Latch. In the Reset phase the latch, shown by the back to back inverters, is shorted to ground through M6 and M7. To stop current flowing through the shorted inverters M5 is turned off. Notice that both operations are accomplished by a transition on CLK from low to high. This resets the output of the comparator to zero and place INV1 and INV2 in a known state. For the comparator to work properly it is important that INV1 and INV2 are reset to a known state, any unintentional imbalance between the two inverters might tip the comparator towards one side.

When the clock goes from high to low we enter the Latch phase. In this phase the inverters are connected in a positive feedback loop. What way the latch will swing is controlled by an intentional imbalance in the supply to the inverters. This imbalance is controlled by the transistors M1-M4. Depending on their gate voltages transistors M1-M4 have variable on-resistance. For the moment we will ignore transistors M2 and M3. If M1 and M4 are matched, their on-resistances will be the equal when the differential input voltage (V_{INPUT}) is zero (VIN = VIP). When V_{INPUT} is negative (VIN > VIP) M4 will turn more off, and the resistance in M1

will be lower than resistance in M4. Thus INV1 will be slightly faster than INV2, and the comparator will settle to VOP equals zero and VON equals one. The opposite will occur if the V_{INPUT} is positive (VIP > VIN). Notice that this comparator does not need multiple clocks or inverted clocks, one clock signal is sufficient to trigger transition from one phase to another and back again.

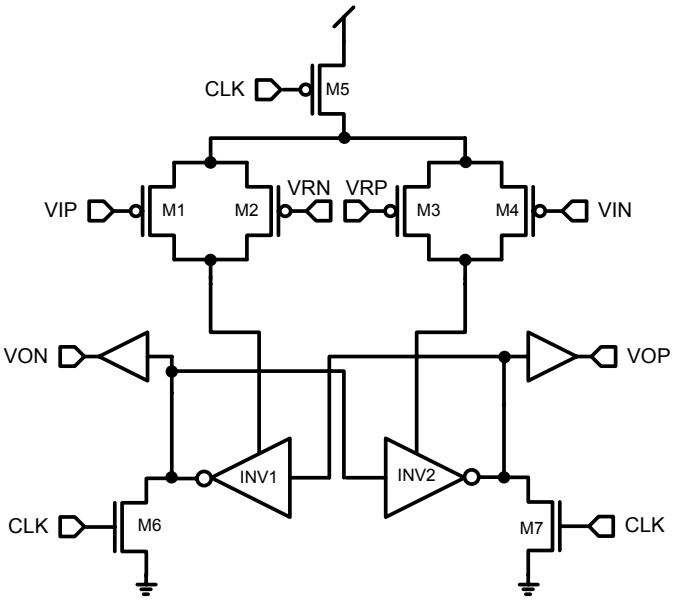

Figure 7.1: Dynamic comparator

As stated, with M2 and M3 ignored the comparator has a threshold at $V_{INPUT} = 0$. However, in a 1.5-bit pipeline stage we need two comparators with the thresholds given by eqs. (7.2) and (7.3) [36]. The transistors M2 and M3 serve to offset the threshold of the comparator. They add small amounts of current to the two branches and intentionally tip the balance of the comparator. Ideally we would scale M2 and M3 to one fourth of the width of M1 and M4. However, as we will se later, this is different in a real process.

$$V_{INPUT} = +\frac{1}{4}V_{REF} \tag{7.2}$$

$$V_{INPUT} = -\frac{1}{4}V_{REF} \tag{7.3}$$

We have two reference voltages, high and low. These are common mode plus V_{REF} and common mode minus V_{REF}, respectively. With the high and low reference voltages connected to VRP and VRN, respectively, the threshold will be set at (7.2) . If we reverse the connections to VRP and VRN we set the threshold at (7.3) .

The boundary conditions for the inverters play an important role in deciding which way the comparator swings. If we have large difference in e.g. the capacitive load at the output of the inverters the comparator might swing the wrong way. Therefore, we keep the load controlled by using two matched buffers at the output of the inverters. We have chosen a high reference at 0.6V and a low reference at 0.2V. The common mode is set at 0.4V. Thus, the maximum allowable offset in this work is $\pm V_{REF}/4 = \pm 0.2V/4 = \pm$ 50mV. Simulations will show that the comparator stays within this limit.

Mismatch between transistors can influence the offset of the comparator. Mismatch of MOSFET transistors can be reduced by increasing the area of the transistor [38]. We tried to keep transistor areas as large as possible in order to reduce mismatch, while small enough to keep capacitances low. All transistors have a length of 0.1μm to maximize the speed, according to (7.1). All PMOS devices have a width of 3μm and all NMOS devices have a width of 1.2μm as seen in Table 7.1. Devices are kept at the same width to simplify layout to maximizing the matching [4]. Notice that the effective width, width x Number of Unit Devices in parallel (NUD), of M1 and M2 does not correspond to a scaling of one-fourth. In the 90nm process we are using a scaling of eight was necessary to keep the threshold at the reasonable level. M6 and M7 are the twice the effective width of the NMOS transistors in the inverters.

7.3 Simulation Results

Some of the key parameters for this dynamic comparator are offset, delay and power dissipation. The offset needs to be within plus/minus one-fourth

Table 7.1: Transistor widths and fingers. [1]NUD: Number of Unit Devices in parallel

Transistor	**Width (μm)**	**NUD**[1]
M1 & M4	3.0	16
M2 & M3	3.0	2
M5	3.0	84
M6 & M7	1.2	2

of the reference voltage, which in our case corresponds to ±50mV. We aimed for a speed of 1GHz at 0.8V. This corresponds to a maximum delay of 500ps from CLK goes low to output is valid. Remember that the comparator has two phases; Reset and Latch, they need 500ps each at 1GHz clock frequency with a 50% duty cycle. We have not considered other duty cycle arrangements.

Since we were primarily considering high speed and low voltage, we did not set any requirements for power dissipation. However, dynamic comparator power dissipation resembles that of digital gates, which have a power dissipation given approximately by:

$$P = fCV_{DD}^2 + V_{DD}I_0 \tag{7.4}$$

Where f is the output frequency, V_{DD} is the supply voltage, C is the output capacitance and I_0 is the average leakage current [39] . With a low supply voltage and limited capacitance we anticipated reasonable power consumption.

Simulations were performed in five process corners; Fast, Typical, Slow and cross corners (fast NMOS, slow PMOS and visa versa). We also ran three temperature corners (-40^o, 0^o, 85^o) for each process corner. In addition, Monte Carlo simulations were performed to simulate the effect of mismatch. All transistors included a model of gate leakage current. A capacitive load of 100fF was used at the output of the buffers in all simulations. Each parameter (offset, delay and power dissipation) was extracted in each of the corners. Typical values were extracted from typical process

corner. The standard deviation (σ) for power dissipation and offset was extracted from a Monte Carlo simulation. For offset it was around 3 mV for both high and low threshold. For power dissipation the standard deviation was negligible. We subtracted 3σ from the minimum value and added 3σ to the maximum value of offset and power dissipation. Table 7.2 shows the results for comparator offset and power dissipation including 3σ. The offset is within $\pm$25mV which is well below the required $\pm$50mV. The maximum power dissipation was 222μW, almost half of this was dissipated in the output buffers. As previously stated we have used a similar architecture to that of [37]. They achieved 100μW with 200fF at 50Msamples/s and 1V in a 0.25μm CMOS technology. Since most of the power dissipation in this architecture is dynamic we can use (7.4) to compare the two results. If we scale the results from [37] to 1GHz with 100fF and 0.8V we get a power dissipation of 640μW. Thus, a maximum power dissipation of 222μW at 1GHz with 100fF and 0.8V can be considered reasonable.

Simulating delay in a comparator requires that one choose the input signal with care. It can be shown that the delay of latched comparators becomes large when the differential input voltage is close to threshold [4]. We simulated the delay around the threshold by applying a differential ramp at the input from 20mV above the ideal threshold to 20mV below the ideal threshold using 200 clock periods running at 1GHz. The change in input from one clock period to the next was around 200μV. It is difficult to know exactly where the threshold of the comparator is. We therefore used the delay of the second pulse after the comparator switched states. By doing this we know we never measure delay exactly at the threshold, but always within 200μ - 400μV away from the threshold. As with offset and power dissipation, a Monte Carlo simulation was performed to get the σ of the delay. The σ of the delay decreased as we moved away from the threshold. The standard deviation of the delay for the first pulse after threshold was up to 30-50ps for high and low thresholds, most of which we believe is due to varying distance to threshold when the comparator latches. The σ of the delay for the second pulse was below 10ps, it is this σ that has been used in Table 7.2. In the worst corner and including 3σ variation in delay due to

mismatch, the comparator has less than 400ps delay. This would give us a maximum clock frequency of 1.25GHz, but allowing for a safety margin we choose 1GHz as maximum.

If the differential input voltage is closer than $\pm 200\mu$V to the threshold, less than what was used in simulation, there is a chance of metastability. Metastability is when the comparator has larger delay than the available settling time. A detector for metastability can be inserted after the comparator [40]. A XOR port connected to VON and VOP, with delay much smaller than the comparator, will give a one if there is no metastability and zero if there is metastability. This is ensured by the reset to zero of both outputs in the Reset phase. In a case of metastability one can arbitrarily choose output state of the comparator since one knows that the input is close to threshold, much closer than the required $\pm$50mV. However, when using a metastability detector one must make sure that the pull-down delay of Reset plus delay of the detector is less than half the clock period. In this design the pull-down delay in Reset was below 200ps. We have not yet considered effects of layout parasitics.

Table 7.2: Offset, power dissipation and delay

Parameter	**Min**	**Typ**	**Max**	**Unit**
Offset (High threshold)	-22.5	9	15	mV
Offset (Low threshold)	-16	8.5	22	mV
Power diss.@1GHz	180	193	222	μW
Delay	80	186	< 400	ps

7.4 Future work

The comparator is scheduled for production in a digital 90nm CMOS technology during fall of 2005. The main purpose of the prototype is to verify the rather small variations due to process variation and mismatch seen in simulations. If the prototype confirms what has been seen in simulations the comparator will be used in scheduled high performance ADCs.

7.5 Acknowledgements

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7.6 Conclusion

The design of a 0.8V 1GHz dynamic comparator in digital 90nm CMOS technology has been presented. The work shows that low voltage, low power and high speed analog circuits are feasible in nano-scale CMOS technology. The dynamic comparator dissipates a maximum of 222μW at 1GHz clock frequency with 100fF capacitive load at a supply voltage of 0.8V which is lower than comparable results. Table 7.3 shows a summary of simulation results.

Table 7.3: Summary of simulation results

Offset $<\pm$ 25mV	
Clock Frequency	$>$ 1GHz
Power dissipation	$<$ 222μW
Supply voltage	0.8 V
Clock signals	1
High reference	0.6V
Low reference	0.2V
Common mode	0.4V

Chapter 8

Paper 5

Design of a 7-bit 200MS/s, 2mW Pipelined ADC With Switched Open-Loop Amplifiers In a 65nm CMOS Technology

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Abstract

We present the design of a 7-bit 200MS/s pipelined ADC with switched open-loop amplifiers in a 65nm CMOS technology. As a result of turning off the open-loop amplifiers during sampling we reduce the power dissipation by 23%. The ADC achieves a SNDR of 40dB close to the Nyquist frequency, with a power dissipation of 2mW, which results in a Walden FOM of 0.13pJ/step and a Thermal FOM of 1.6fJ/step.

8.1 Introduction

Low resolution high speed ADCs have historically been Flash based architectures. The Flash ADC is a fast architecture due to it's parallel nature.

However, it is a very inefficient architecture. One of the reasons for its inefficiency is that it is not possible, with current processing technology, to get the input capacitance down to what is the minimum required by thermal noise. This is mostly due to parasitic capacitances from transistors and metal routing.

Before we begin our argumentation we should define what we mean with parasitic capacitances. We define parasitic capacitance as; any capacitance that is not required by the operation of the circuit.

One of the fundamental error sources that limit the performance of ADCs is the thermal noise power, which is usually represented as $\overline{V_{thermal}^2} = a \times kT/C$ where a is a constant, k is Boltzmann's constant, T is the temperature in Kelvin and C is the sampling capacitance.

Thermal noise power sets the lower limit for how much power we must dissipate to achieve a certain SNR. With respect to thermal noise power a certain SNR usually translates into a certain sampling capacitance.

If we assume a quantization noise power of $\overline{V_{LSB}^2} = V_{LSB}^2/12 = V_{max}^2/(2^{2bits} \times 12)$, and we assume $\frac{1}{4}\overline{V_{LSB}^2} = \overline{V_{thermal}^2}$ and $a = 1$, the equation for the required sampling capacitor is

$$C = \frac{48kT2^{2bits}}{V_{max}^2} \tag{8.1}$$

If we use 6 bits, $k = 1.38 \times 10^{-23} J/K$, $T = 353K$ and $V_{max} = 0.4V$ the required sampling capacitance is 6fF. This, of course, assumes that other concerns like mismatch or unwanted effects from parasitic capacitances does not come in to play.

Parasitics at a node can reach 10fF in current nanoscale technologies, as a consequence the parasitics can be larger than required sampling capacitor at the 6-bit level. This is one reason why a Flash ADC looses when it comes to efficiency. A 6-bit Flash ADC without averaging or interpolation has 64 comparators connected to the input, each of which has possibly 10fF input capacitance. Thus a Flash ADC can have 600fF input capacitance, which is two orders of magnitude larger than the required sampling capacitance.

If we look at the figure of merit (FOM) of 6-bit ADCs, and higher

resolution ADCs, using the Walden FOM [5] given by

$$FOM = \frac{P_{diss}}{2^{bits} f_s} \tag{8.2}$$

where P_{diss} is the power dissipation and f_s is the sampling frequency. And the Thermal FOM given by

$$FOM = \frac{P_{diss}}{2^{2bits} f_s} \tag{8.3}$$

We get Figure 8.1, with the gray diamonds representing Walden FOM and the black triangles representing Thermal FOM. The data for Figure 8.1 was collected from ADCs published in the Journal of Solid State Circuits in the years 1975-2005. According to the Walden FOM there are 6-bit ADCs that are just as good as the 15-bit ADCs, since they have the same figure of merit. However, the Walden FOM is an empirically deduced FOM, and it has come under some scrutiny in the recent years. A more theoretically correct FOM is the Thermal FOM.[1]

The argument for why the Thermal FOM is more correct is as follows. Assume a thermal noise limited ADC, where the power dissipation is proportional to the sampling capacitance. If we increase the resolution by one bit, we can see from (8.1) that the sampling capacitance quadruples, and through this the power dissipation quadruples. However, the Walden FOM only allows a doubling of the power dissipation for each bit of resolution added. This leads to an unfair FOM for high number of bits and a lenient FOM for low number of bits.

Two alternatives to Flash ADCs have received some attention in recent years. The first is successive-approximation (SAR) ADCs and the second is pipelined ADCs. Both have in recent papers achieved good results.

In [41] they presented a 6-bit 600MS/s time interleaved asynchronous successive-approximation ADC, with a Walden FOM of 0.22pJ/step and a Thermal FOM of 5.7fJ/step. In [42] they presented a 6-bit pipelined ADC with open-loop amplifiers achieving a Thermal FOM of 59fJ/step. Note

[1] As far as we know the FOM has not yet been given a name, so the name Thermal FOM is not an official name. It is, however, a descriptive name.

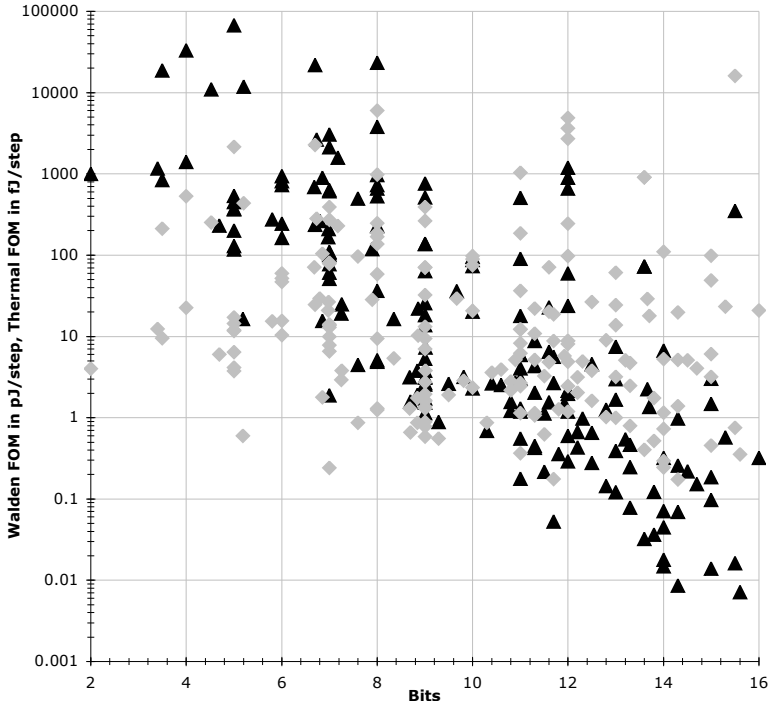

Figure 8.1: Walden FOM versus Thermal FOM as a function of bits for ADCs published in the Journal of Solid State Circuits 1975-2005. Thermal FOM in black and Walden FOM in gray.

that the best 6-bit ADC in Figure 8.1, is [43] with a Thermal FOM of 16.38fJ/step, which is three orders of magnitude worse than the best $>$ 14-bit ADCs. And the best 7-bit ADC is a 100kS/s SAR [44] with a Thermal FOM of 1.89fJ/step, which is two orders of magnitude worse than the best $>$ 14 bit ADCs.

Our goal for this design was to optimize the FOM for a low resolution ADC at a resonable speed. We choose to design a pipelined ADC and placed it at the conservative speed of 200MHz. That is, the speed is conservative if we compare to the speed to [42] or [41]. Usually, low resolution ADCs are used in the GHz range, so we assume that the this pipelined ADC would be used in a time interleaved architecture. Knowing that we would be unable to use a 6fF sampling capacitor we opted for 7-bit resolution, since the thermal noise power would anyway be low because of the larger sampling capacitor,

and adding one more stage does not increase the power significantly. To keep parasitic capacitances from transistors as low as possible we chose to use a 65nm CMOS technology. The pipelined ADC architecture is explained in the following section with results of simulations presented in Section 8.3.

8.2 Pipelined Architecture

The ADC was designed in a 65nm low power CMOS technology with low threshold voltage (lvt) transistors. The architecture of the differential pipelined ADC is shown in Figure 8.2. The ADC has five 1.5-bit pipelined stages and a three level flash at the end. Each stage has a three level analog to digital converter (SADC) and a multiplying DAC (MDAC). The MDAC has a gain of two.

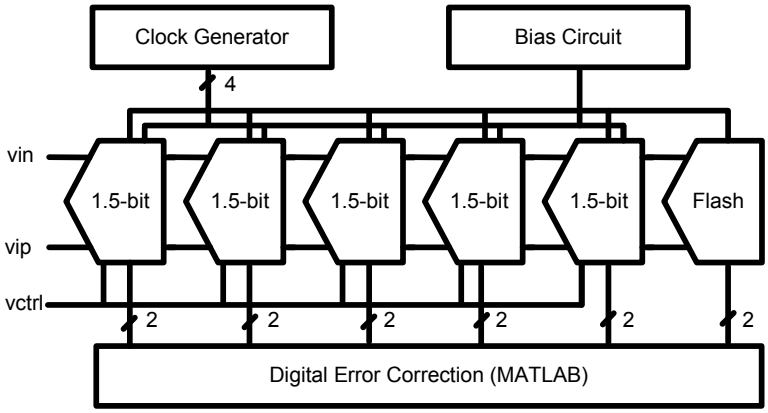

Figure 8.2: Architecture overview of the 7-bit Pipelined ADC with open-loop amplifiers

One of the alternatives to the traditional operational amplifiers in MDACs is an open-loop amplifier, like a common source amplifier, with a gain of two. This technique has been used with success in a 12-bit pipelined ADC [45] and 6-bit pipelined ADC [42]. Our design is based on [42]. The MDAC architecture can be seen in Figure 8.3. Figure 8.3 shows stage one and stage two. Stage one is in the amplifying phase, the SADC has made its decision, and the control signals t0, t1 and t2 control transmission gates that con-

nect one of the two sampling capacitors to high reference, common mode or low reference. The control signals t0, t1, t2 and the transmission gates implement the DAC. Stage two is shown in the sampling phase. Here both capacitors are connected to the input through transmission gates controlled by clock ip1. Each stage needs three clock phases, p1, p1a and p2, where p1a is slightly advanced over p1, and is used to sample the input when it is quiet. p1 and p2 are non-overlapping clock phases. Stage two uses ip1, ip1a and ip2, where ip1=p2 and ip2=p1. All in all we need four clock phases for the complete pipelined ADC, p1, p1a, p2 and p2a. The open-loop amplifier is marked by x2 in Figure 8.3.

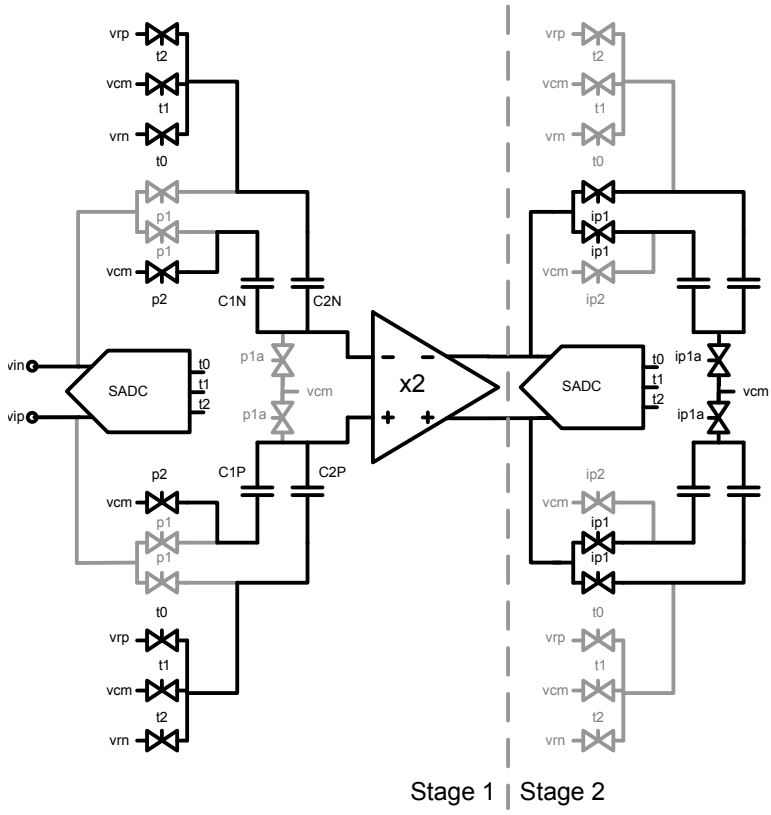

Figure 8.3: Stage 1 and stage 2 in the pipelined ADC

8.2.1 Open-Loop Amplifier

A detailed schematic of the open-loop amplifier can be seen in Figure 8.4. It is a differential common source amplifier with resistive load. The resistors are each $4k\Omega$, and we assume that they will be calibrated at startup, so the resistor value is constant over process. In this differential amplifier it is important that the common mode variation is low. If not, the common mode voltage will drift as the signal propagates through the pipelined stages, and may even turn later stages off. To achieve low common mode variation we use a replica bias that keeps the total current, $I_{tot} = I_{R1} + I_{R2}$, equal to two times I_{bias} over process, voltage and temperature variations. Through this the common mode voltage is determined by $V_{cm} = V_{dd} - I_{tot}/2 \times (R1 + R2)/2$ which keeps it constant over process and temperature variation.

The transistors M5/M6/M1/M2 are twice the size of M7/M8/M11/M12, as a consequence $I_{tot} = 2I_{bias}$. We choose the common mode to be 0.6V, to get larger overdrive on the input transistors, and the swing to be $\pm 0.2V$.

The gain of the common source amplifier, if we disregard the source degeneration, is given by $A_o = g_{m1}R_1$ The gain will vary over process and temperature because of changes in g_m, we compensate for some of this change by varying the vctrl voltage of the source degeneration transistor, which in effect changes the effective source degeneration resistor and in turn changes the gain of the amplifier. If we include the source degeneration the gain expression becomes

$$A_o = \frac{g_{m1}R_1}{1 + \frac{g_{m1}}{2g_{ds13}}} \tag{8.4}$$

In [42] they used a replica MDAC stage configured in a feedback loop to control the vctrl voltage such that the MDAC stage has a gain of two. Since we only do simulation we have not included the replica stage, the vctrl voltage is changed manually for each corner simulation.

The gain of the MDAC is also affected by the input capacitance of the amplifier as described in [42].

Our main contribution to reduce the power of the pipelined ADC is the transistors M3/M4, these turn off the the amplifier during sampling phase when it is not needed. Because the drain and source nodes of M3/M4 are

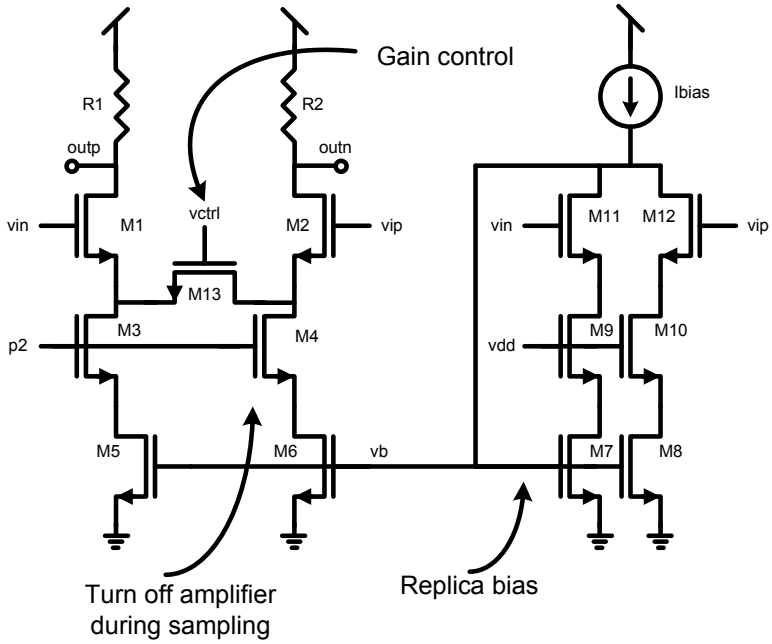

Figure 8.4: Open-Loop Amplifier

low impedance, and the bias voltage, vb, stays constant, the amplifier turns on quickly.

In our design the bias current is $I_{bias} = 100\mu A$, which makes the total current consumption of a MDAC stage $300\mu A$, ergo the power dissipation of five MDAC stages should be $1.5mW$, assuming we use a 1V supply. This is if we leave the amplifiers on all the time. By turning off the amplifiers during sampling the power dissipation is reduced to $P_{mdacs} = 5 \times 100\mu A \times 1V + \frac{1}{2}5 \times 200\mu A \times 1V = 1mW$, so we would expect an improvment of 0.5mW when the amplifiers are turned off during sampling.

With this low current in the amplifiers, the input capacitance of the next stage must be low. The sampling capacitors (C1, C2) are chosen at 50fF. The reason for choosing such a large value compared to the required, is not capacitor matching concerns, which do not come in to play at 7-bit, but rather the parasitic capacitance from the amplifier input, which reduces the gain of the MDAC. We compensate for some of this reduction in gain with the vctrl voltage.

Two other circuits dissipate power in the pipelined ADC, the SADCs and the clock generator/buffers. The size of the clock buffers are mainly determined by the load of the SADCs and routing capacitance. The power dissipation in the SADCs are determined by matching concerns of the comparators. The comparators used are the so called Lewis-Gray dynamic comparators introduced in [35].

8.2.2 Clock Generation

Most switched capacitor circuits use two non-overlapping clocks to control the charge transfer, but since we use bottom plate sampling there is an advanced phase 1 that transitions just before phase 1. The advanced clock phase reduce the problem of input dependent charge injection from the input switches.

We use NMOS inputs in the comparators due to the high common mode voltage, thus the comparators use a clock that samples on the rising edge. To avoid distributing inverted clock phases we invert the clocks of the transmission gates, which means that the transmission gates are on when the clock signal is low, and off when the clock signal is high. The clock buffers were scaled to drive 6 SADCs, transmission gates, amplifier turn-off control signal and a 100fF capacitance was added at the output of each clock buffer to model the the parasitic capacitance added by metal routing.

8.3 Results of Simulation

The ADC was simulated at transistor level using Eldo from Mentor Graphics. A common mode of 0.6V, and a swing of 0.2V, as previously mentioned, resulted in a differential peak to peak of 0.8V with a 1V supply. Both the references and inputs are assumed to be buffered off-chip, the buffers are not included in the simulation. Results of Eldo simulations were post-processed in MATLAB, were an FFT was performed and signal-to-noise-and-distortion (SNDR) was extracted. In all simulations an input signal frequency close to the Nyquist frequency was used, and an input signal amplitude of 0.8 times full scale range.

Mismatch simulations were performed in the typical corner at a temperature of 27 degrees Celcius. A 2^7 point FFT was used to estimate the SNDR and 101 simulations were run to get an estimate of the standard deviation of the SDNR due to mismatch. The mean SNDR was 40dB and the standard deviation was 1.2dB.

Four process corners (fast, slow, fast-slow, slow-fast) and three temperature corners $(0^o, 27^o, 80^o)$ were simulated. When we vary vctrl to compensate for the threshold voltage changes, the standard deviation in SDNR over process corners and temperature corners is 2.35dB, with the worst corner being slow process and low temperature. With constant vctrl the standard deviation increases to 3.45dB.

Figure 8.5 shows an 2^{10} point FFT of the output from a transient simulation with noise in the typical corner.

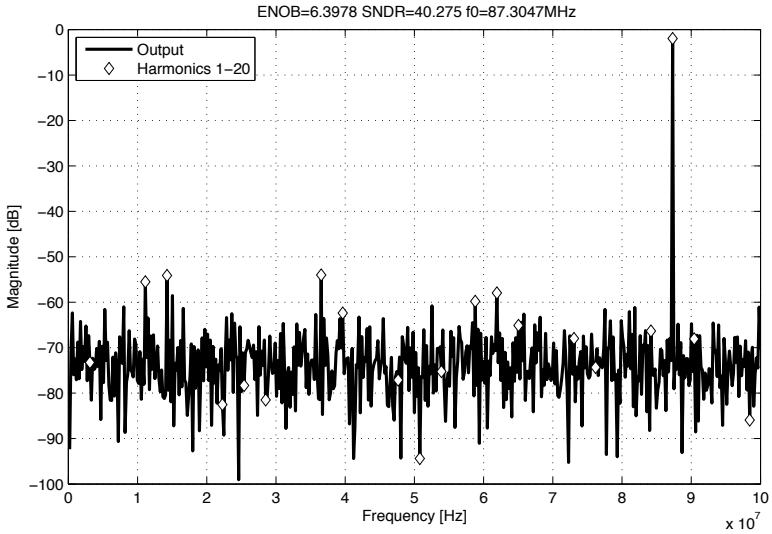

Figure 8.5: A 1024 point FFT of the ADC output from a transient noise simulation. The harmonics of the fundamental are marked with diamonds.

The total power dissipation for the simulated ADC in typical corner (typical process, 27^o and 1V supply) is 2mW. If we leave the amplifiers turned on during sampling it dissipates 2.6mW, with the increase being close to the expected 0.5mW. Table 8.1 summarizes the achieved performance in

the typical corner.

The Walden FOM of the ADC is 0.13pJ/step and the Thermal FOM of 1.6fJ/step. The improvement is almost a factor four compared to the Thermal FOM of 5.7fJ/step from [41], bearing in mind that they have proven silicon, and that the difference might be eaten up by layout parasitics. In addition, we operate at a lower speed and a higher SNDR, which makes it more straightforward to achieve a good figure of merit. However, [41] was a SAR while our ADC is a pipelined ADC, making the point the two architectures can compete on equal grounds with respect to figure of merit at reasonable speeds.

Table 8.1: Preformance summary of the 7-bit Pipelined ADC

Technology	65nm LP CMOS
Input Voltage Peak-to-Peak	0.8V
Supply Voltage	1V
Sampling Frequency	200MHz
SNDR	40dB
ENOB	6.3dB
Power Dissipation	2mW
Walden FOM	0.13pJ/step
Thermal FOM	1.6fJ/step

8.4 Future Work

Low resolution pipelined ADCs with open-loop amplifiers make for an interesting architecture, it may well be the most efficient, straightforward way to implement high speed low resolution ADCs at the present time. More work is needed to try to reduce the sampling capacitance, and we believe that cutting the parasitic capacitances down, through architecture or technology changes, is the most effective way to increase effectiveness of high speed low resolution ADCs.

8.5 Conclusion

We presented the design of a 7-bit 200MS/s pipelined ADC with switched open-loop amplifiers in a 65nm CMOS technology. As a result of turning off the open-loop amplifiers during sampling the power dissipation was reduced by 23%. The ADC achieved a SNDR of 40dB close to the Nyquist frequency, with a power dissipation of 2mW, which resulted in a Waldon FOM of 0.13pJ/step and a Thermal FOM of 1.6fJ/step.

Acknowledgments

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Chapter 9

Paper 6

Design and Behavioral Simulation of Comparator-Based Switched Capacitor Circuits

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Accepted at 26th NORCHIP Conference 2008

Errata

- Section 9.7, third paragraph, fifth line: 11% should be 16%

Abstract

Design equations are a required tool in the analog designers toolbox. In this paper we show how one can calculate the required parameters for comparator-based switched-capacitor circuits for use in a pipelined ADC. The parameters are capacitance (C), current (I_0), comparator delay (T_d), current source output resistance (R_o) and comparator threshold (V_{ct}). The design equations are verified with behavioral simulations in SPICE and MATLAB.

Keywords Comparator-based switched-capacitor circuits, design equations, pipelined analog-to-digital converters

9.1 Introduction

Downscaling of CMOS technology continue to challenge the analog designer. Reduced power supply, due to reliability concerns [31], and reduced transistor output resistance, due to shorter channels [32], lead to low headroom and low intrinsic gain. As a consequence, high DC gain operational amplifiers (opamp) — the key component in most switched-capacitor circuits — is hard to design in nano-scale technologies.

Techniques like correlated level shifting [46], open-loop residue amplifiers [45], gain calibration [47], and comparator-based switched-capacitor circuits (CBSC) [48] have been developed to solve some of the challenges. The techniques either reduce the gain requirements for a given resolution, or replace the opamp completely.

Introduced in [48] CBSC is a completely new approach to switched-capacitor circuits. It replaces the opamp with a comparator and a current source. To demonstrate the technique a prototype 10-bit 8-MS/s 2.5-mW pipelined ADC was presented at ISSCC 2006 [48]. The implementation was detailed in [49].

In this paper we discuss how to design CBSC circuits for analog-to-digital converters.

Before one starts simulating transistors in SPICE it is of utmost importance to have a clear idea of the dominating error sources, and how they should be handled. In that respect, tools like design equations, mathematical simulations and behavioral SPICE simulations are invaluable tools for the analog designer.

Design Equations Based on the specification (how fast, how accurate, how little power) the parameters for different circuit blocks can be calculated. The design equations result in a place to start, a set of initial parameters to work with.

Mathematics based simulation Behavioral simulation in a mathematics based tool, like MATLAB or OCTAVE, is more complex than design

equations, but more accurate. But it is still fast and a designer can sweep parameters to find optimal solutions.

SPICE simulation Behavioral level description in SPICE allow the designer to have a top-level description of the circuit, with all circuit blocks defined. The functionality of circuit blocks is checked before circuit blocks are implemented with transistors.

This paper is organized as follows: Section 9.2 review opamp based switched-capacitor circuits. Section 9.3 explain comparator-based switched-capacitor circuits. A model of the output voltage of a CBSC amplifier with a gain of two is described in Section 9.4. In Section 9.5 we introduce a design methodology for CBSC circuits and show a design example in Section 9.6. Results of simulations in MATLAB and SPICE verify our design equations in Section 9.7.

9.2 Opamp based switched-capacitor circuits

Switched-capacitor (SC) circuits are usually designed with an opamp feedback loop as shown in Fig. 9.1. Most SC circuits have two clock phases, sampling and charge transfer. Fig. 9.1 is a amplifier where the input is sampled in phase p_1, and charge is transferred from C_1 to C_2 in p_2 by forcing V_x to ground. If the opamp has infinite gain the discrete time transfer function for Fig. 9.1 is a delayed amplification, where the gain is determined by the capacitance ratio.

$$H_0(z) = \frac{C_1 + C_2}{C_2} z^{-1} \tag{9.1}$$

With finite gain in the opamp the transfer function is

$$H_1(z) = H_0(z) \times \frac{1}{1 + (C_1/C_2 + 1)/A} \tag{9.2}$$

where A is the DC gain of the opamp. Finite gain in the opamp reduce the gain of the SC amplifier. For the remainder of this work we assume $C_1 = C_2$, so the amplifier has a gain of two.

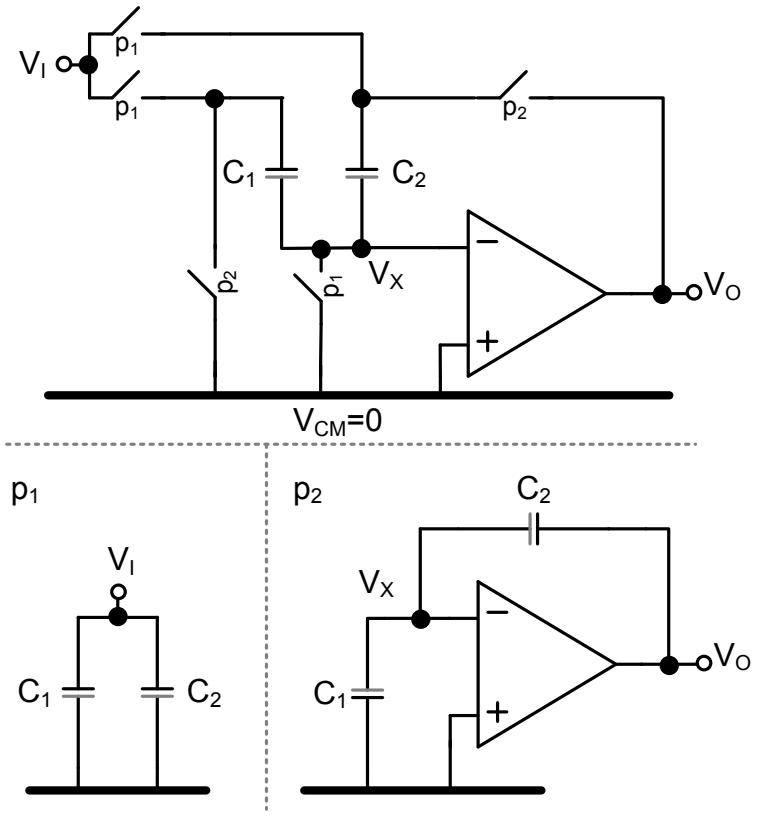

Fig. 9.1: Switched-capacitor amplifier using an operational amplifier

9.3 Comparator-based switched-capacitor circuit

It does not matter how a SC circuit arrive at the output voltage. What matters is that the output voltage is correct when the next stage samples, which usually is at the end of charge transfer.

Instead of an opamp a current source and a comparator can be used [48]. An opamp forces the virtual ground condition while CBSC charge the output with a current source and detect when virtual ground is reached.

An example of a single ended CBSC is shown in Fig. 9.2, only charge transfer phase is shown, sampling phase is equivalent to opamp based SC.

At the start of charge transfer the output is reset to the lowest voltage in the system (usually the negative supply voltage), which ensure that V_x start below the virtual ground (common mode). The current source is turned on at the start of reset and use reset to settle. When reset ends the current source charge the output capacitance. The voltage at V_o and V_x rise until the comparator detects virtual ground ($V_x = V_{CM} = 0$). Due to the comparator delay it takes a moment for the current source to turn off, which result in an overshoot.

The overshoot can be corrected in several ways. One way is using two ramps [48], one fast and one slow, the fast ramp does an estimate of the output voltage, while a slow ramp in the opposite direction discharge the overshoot. Another is to change the threshold of the comparator to compensate for the overshoot [50].

A analytical model of the output voltage is presented in the next section.

9.4 Model of CBSC output voltage

Assume finite resistance in current source. Kirchhoff's current law give the differential equation

$$I_0 = C_o \frac{dV_o(t)}{dt} + V_o(t)/R_o \tag{9.3}$$

where C_o is the capacitance at the output, V_o is the output voltage, I_0 is the current in the current source and R_o is the output resistance of the current

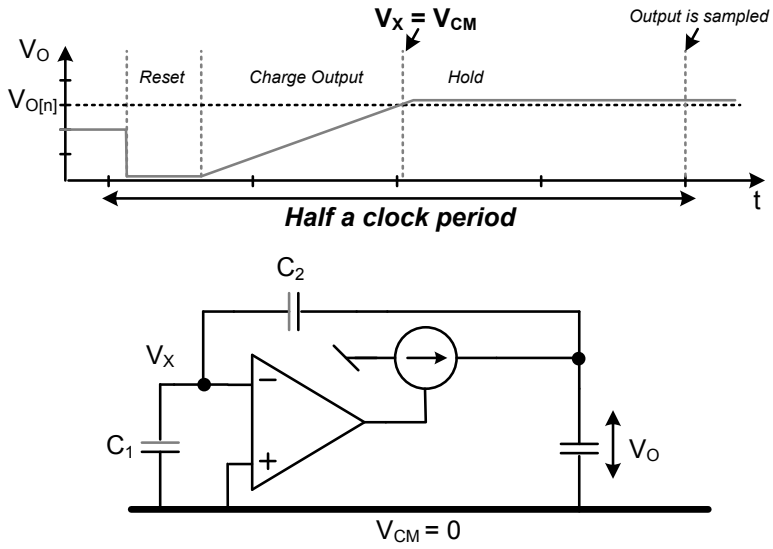

Fig. 9.2: Comparator-based switched-capacitor circuit

source. Solving the differential equation yields.

$$V_o(t) = I_0 R_o \left(1 - e^{-\frac{t}{R_o C_o}}\right) \tag{9.4}$$

The time t is the sum of T_{V_I} — the time to charge to the ideal output voltage ($V_o(t) = 2V_I$) — and the comparator delay T_d. The ideal charge time T_{V_I} is given by

$$T_{V_I} = -ln\left(\frac{-2V_I}{R_o I_0} + 1\right) C_o R_o \tag{9.5}$$

To compensate for the comparator delay the comparator threshold (V_{ct}) can be changed, so the comparator start switching before $V_o = 2V_I$ is reached. Accordingly, the charge time can be written as

$$t = -ln\left(-2\frac{V_I - V_{ct}}{R_o I_0} + 1\right) C_o R_o + T_d \tag{9.6}$$

Inserting (9.6) in (9.4) results in

$$V_o(t) = 2e^{-\frac{T_d}{R_oC_o}}V_I + I_0R_o[1 - e^{-\frac{T_d}{R_oC_o}}(1 + 2\frac{V_{ct}}{I_0R_o})] \tag{9.7}$$

The gain in of the amplifier should be two, but from (9.7) we see the gain is smaller than two ($2e^{-T_d/R_oC_o}$).

This gain error will cause static non-linearities when a CBSC circuit is used in a pipelined ADC. The gain error is a function of the comparator delay, the output resistance and output capacitance. The last term in (9.7) is the overshoot.

In the next section we will use these equations to calculate the necessary parameters for a CBSC circuit.

9.5 CBSC design equations

The SC circuit in Fig. 9.2 finds use in pipelined ADCs in the multiplying digital-to-analog converter (MDAC) [51]. The necessary parameters for CBSC are capacitance (C), current source current (I_0), comparator delay (T_d), current source output resistance (R_o), and comparator threshold (V_{ct}).

The first thing we need to calculate is the necessary sampling capacitance given by [52]

$$C = a_1 \times \frac{48kT2^{2B}}{V_{PP}^2} \tag{9.8}$$

where a_1 is a constant larger than one, k is Boltzmann's constant, T is the temperature in Kelvin, B is the number of bits, and V_{PP} is the differential peak-to-peak signal swing.

To estimate the required current we assume that the output ramp is constant so

$$V_o = \frac{I_0}{C_o}t \tag{9.9}$$

The current in the current source is then calculated from

$$I_0 = \frac{C_o(V_{pp}/4 + V_{cm})}{\frac{1}{2f_s} - T_r} \tag{9.10}$$

where V_{cm} is the common mode voltage, f_s is the sampling frequency, T_r is the reset time and C_o is the output capacitance given by

$$C_o = \frac{C_1 C_2}{C_1 + C_2} + C_L \tag{9.11}$$

where $C_1 = C_2 = C/2$, and C_L is the capacitance of the next stage.

The comparator delay is chosen based on technology and noise properties [49].

The required output resistance of the current source is determined by the gain error from (9.7)

$$1 - \epsilon_g = e^{-T_d/R_o C_o} \tag{9.12}$$

where ϵ_g is the gain error. The required output resistance is then

$$R_o = \frac{-T_d}{ln(1-\epsilon_g)C_o} \tag{9.13}$$

The comparator threshold (V_{ct}) compensate for the overshoot from (9.7) given by

$$V_{off} = I_0 R_o \left[1 - e^{-\frac{T_d}{R_o C_o}} \left(1 + 2\frac{V_{ct}}{I_0 R_o} \right) \right] \tag{9.14}$$

Hence, the comparator threshold can be calculated from

$$V_{ct} = -1/2\, I_0\, R_o \left(1 - e^{\frac{T_d}{R_o C_o}} \right) \tag{9.15}$$

9.6 Design example

As an example we use a 9-bit pipelined ADC running at 50MS/s. The target technology is 90nm CMOS with a power supply of 1.2V, the signal swing is 1V peak-to-peak differential.

The comparator in the CBSC circuit is the dominating noise source, and according to [49] it adds slightly more than two times the noise power of a single transistor. We choose $a_1 = 3$ to have some margin. With $T = 300K$ the capacitance is from (9.8)

$$C = 160fF \tag{9.16}$$

The current, calculated from (9.10), is

$$I_0 = 22\mu A \tag{9.17}$$

where we have used $V_{cm} = 0.6V$, a reset time of $T_r = 1ns$ and $f_s = 50MHz$. Allowing for a margin we choose $I_0 = 30\mu A$.

The current is proportional to C_o, which is highly process dependent parameter (20% variation). To rectify this a capacitance dependent bias current could be used [51].

The comparator delay (T_d) depend on implementation, but in 90nm CMOS a delay of half a nanosecond is possible.

$$T_d = 0.5ns \tag{9.18}$$

The size of the gain error is a design choice. Using an ideal pipelined model in MATLAB we deduced that a gain error of $\epsilon_g = 1/2^B$ results in a 0.1dB reduction in signal-to-noise and distortion ratio (SNDR) and a spurious free dynamic range (SFDR) of 65dB. The output impedance of our current sources can then be calculated from (9.13)

$$R_o = 1.1M\Omega \tag{9.19}$$

From (9.15) the comparator threshold offset is

$$V_{ct} = 32mV \tag{9.20}$$

We now have the parameters we need for a behavioral level model. The next section verify the design equations with behavioral simulations in MATLAB and SPICE.

9.7 Simulation results

The simulated ADC is a 9-bit pipelined ADC with 1.5-bits per stage. In the MATLAB model the MDAC is modeled by (9.7). In the SPICE model the MDAC is modeled as shown in Fig. 9.2 with the addition of a resistor in parallel with the current source to model the output resistance.[1]

The parameters are summarized in Table 9.1. In all simulations we have used an input signal of -1.9dB. For an ideal converter this reduces the effective number of bits (ENOB) by 0.3-bit.

Table 9.1: Summary of calculated parameters

Technology target	90nm CMOS
Supply voltage	1.2 V
Resolution	9 bits
Full scale input	1V
Sampling frequency	50MS/s
I_0	30μA
T_d	0.5ns
T_r	1ns
$C/2$	80fF
R_o	1.1MΩ
V_{ct}	32mV

[1]Both models can be downloaded from `http://www.wulff.no/carsten` under *Electronics*, *Tools & Scripts*, *Behavioral simulation of comparator-based switched-capacitor circuits*

A comparison between the design equations, MATLAB model and SPICE model can be seen in Table 9.2. There is a good match between the MATLAB model, the SPICE model, and the design equations. For SNDR and SNR there is less than 7% difference. For SFDR there is a difference of 1.3dB between SPICE and MATLAB, which corresponds to a 11% difference. We believe the reduced SFDR in SPICE simulation is due to effects not modeled in MATLAB, like switch resistance, but this has not been confirmed.

A 2048 point FFT was calculated from the outputs of the SPICE and MATLAB models to calculate the SNDR, SNR and SFDR. Coherent sampling and a Hanning window was used to avoid spectral leakage of the fundamental. The FFT of the SPICE simulation is shown in Fig. 9.3. The FFT of the MATLAB simulation is shown in Fig. 9.4. The third harmonic dominate in both FFTs, but there are more spurs in the SPICE simulation.

Table 9.2: Result of simulation

Parameter	Design Eq.	MATLAB	SPICE
ENOB	8.6dB	8.6dB	8.5dB
SNDR	53.4dB	53.5dB	53dB
SNR	53.4dB	53.8dB	53.4dB
SFDR	-	67.3dB	66dB

9.8 Conclusion

Design equations are a required tool in the analog designers toolbox. In this paper we showed how one can calculate the required parameters for comparator-based switched-capacitor circuits for use in a pipelined ADC. The parameters are capacitance (C), current (I_0), comparator delay (T_d), current source output resistance (R_o) and comparator threshold (V_{ct}). The design equations were verified with behavioral simulations in SPICE and MATLAB.

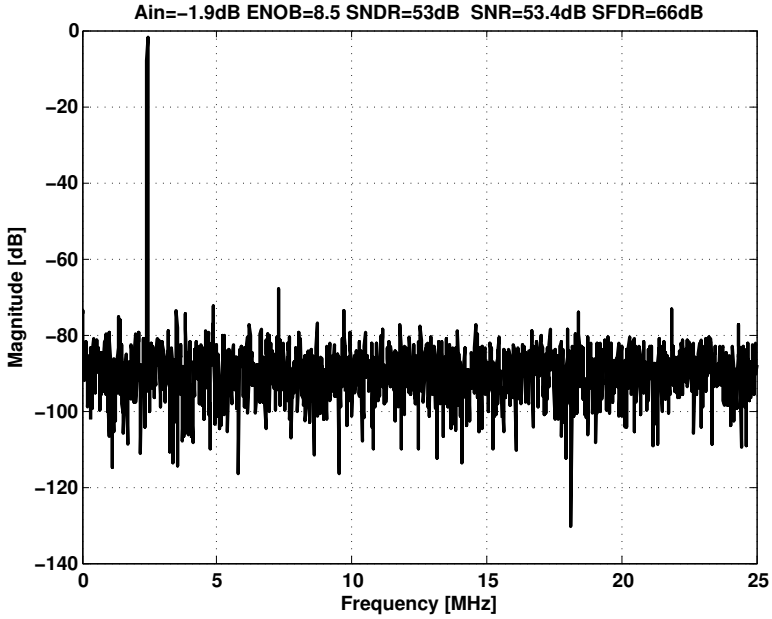

Fig. 9.3: 2048 point FFT of output from SPICE simulation

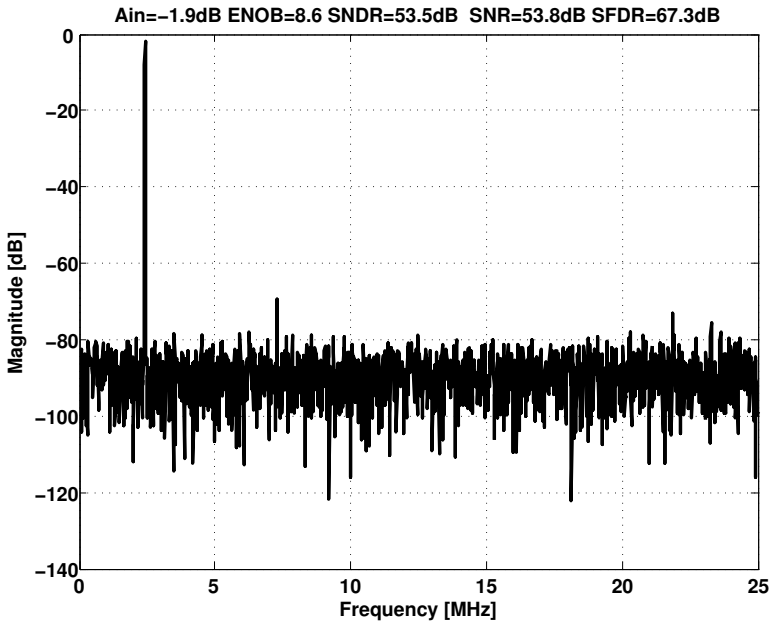

Fig. 9.4: 2048 point FFT of output from MATLAB simulation

Chapter 10

Paper 7

An 8-bit 60-MS/s 8.5mW Differential Comparator-Based Switched-Capacitor Pipelined ADC in 90nm CMOS Technology

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Submitted to Journal of Solid State Circuits

Errata

- INL & DNL: It was later discovered that the INL and DNL was calculated with far to few points, and as a result, contained significant noise. With the current number of points there is a 95% confidence level of a DNL error of 0.4LSB.

Abstract

We present the first differential *comparator-based switched-capacitor* (CBSC) pipelined ADC. The switched-capacitor *multiplying digital-to-analog converter* (MDAC) use current sources and a comparator to do charge transfer. Continuous time bootstrapped switches are used in the first stage to reduce signal dependent switch resistance. A simple calibration algorithm correct for comparator delay variation due to manufacturing. Calibration reduces

ramp overshoot, which dominate the non-linearity in CBSC ADCs. The ADC is produced in a 90nm low-power CMOS technology. The ADC core is 0.85mm x 0.35mm, with a 1.2V supply for the core and 1.8V for the input switches. The ADC has an effective number of bits (ENOB) of 7.05-bit, and a power dissipation of 8.5mW at 60MS/s.

Keywords Comparator-based switched-capacitor circuits, analog-to-digital, pipelined analog-to-digital converters

10.1 Introduction

Downscaling of CMOS technology continue to challenge the analog designer. Reduced power supply, due to reliability concerns [31], and reduced transistor output resistance, due to shorter channels [32], lead to low headroom and low intrinsic gain. As a consequence, high-gain operational amplifiers (opamp)—the key component in most switched-capacitor circuits—is hard to design in nano-scale technologies.

Techniques like correlated level shifting [46], open-loop residue amplifiers [45], gain calibration [47,53], and comparator-based switched-capacitor circuits (CBSC) [48] have been developed to either make the opamp easier to design, or replace the opamp completely.

Introduced in [48] CBSC is a completely new approach to switched-capacitor circuits. It replaces the opamp with a comparator and a current source; to demonstrate the technique a prototype 10-bit 8-MS/s 2.5-mW pipelined ADC was presented at ISSCC 2006 [48]. A year later a 200-MS/s 8-bit 8.5-mW Zero-Crossing-Based pipelined ADC, which replaced the comparator with a zero-crossing detector, was presented [54]. These implementations were detailed in [49] and [50].

Both prototypes were single ended implementations. Single ended ADCs suffer under greater sensitivity to power supply noise and lower signal swings compared to a differential ADC.

We present a differential implementation of a CBSC ADC, and to the

best of our knowledge, it is the first silicon proven differential CBSC. Although, simulation results of a pseudo-differential CBSC sigma-delta is detailed in [55].

The paper is organized as follows: Section 10.2 summarize opamp based switched-capacitor circuits. Section 10.3 explain the CBSC circuits and detail a model of the output voltage of a CBSC MDAC. The circuit implementation is explained in Section 10.4. Calibration of the ADC is presented in Section 10.5 and in Section 10.6 we present the measurement results.

10.2 Opamp based switched-capacitor circuits

Switched-capacitor (SC) circuits are prevalent in pipelined ADCs because of their robustness and accuracy. Doing arithmetic operations like summation, subtraction, and amplification is possible in SC circuit with high accuracy. The accuracy of SC circuits is limited by capacitor matching, which can be accurately set in integrated circuits (on the order of 0.1 percent [4, page 185]).

SC circuits are usually designed with an opamp feedback loop as shown in Fig. 10.1(a). Most SC circuits have two clock phases, sampling and charge transfer.

Fig. 10.1(a) is an amplifier where the input is sampled in phase p_1, and charge is transferred from C_1 to C_2 in p_2 by forcing V_x to ground. If we assume the opamp has infinite gain the discrete time transfer function for Fig. 10.1(a) is a delayed amplification of the input signal

$$H_0(z) = \frac{C_1 + C_2}{C_2} z^{-1} \tag{10.1}$$

where the gain is determined by the capacitance ratio.

With finite gain in the opamp the transfer function is

$$H_1(z) = H_0(z) \times \frac{1}{1 + (C_1/C_2 + 1)/A} \tag{10.2}$$

where A is the DC gain of the opamp. For the remainder of this work we assume $C_1 = C_2$, so the amplifier has a gain of two.

Finite gain in the opamp reduce the gain of the SC amplifier. Normally a gain error is not a significant problem, but in pipelined ADCs a gain error in the MDAC cause static non-linearities, which reduce the accuracy of the converter.

10.3 Comparator-based switched-capacitor circuits

It does not matter how a SC circuit arrive at the output voltage. What matters is that the output voltage is correct when the next stage samples, which usually is at the end of charge transfer.

Instead of an opamp a current source and a comparator can be used to do charge transfer [48]. An opamp forces the virtual ground condition while CBSC charge the output with a current source and detect when virtual ground is reached. An example of a single ended CBSC is shown in Fig. 10.1(b), only charge transfer phase is shown, sampling phase is equivalent to opamp based SC.

First, the output is reset to the lowest voltage in the system (usually the negative supply (VSS)). This ensures that V_X start below the virtual ground (common mode). The current source is turned on at the start of reset and use reset to settle. When reset ends the current source charge the output capacitance. The voltage at V_o and V_X rise until the comparator detect virtual ground ($V_X = V_{CM} = 0$). Due to the comparator delay it takes a moment for the current source to turn off, which results in a overshoot.

The overshoot can be corrected in several ways. One way is using two ramps [48], one fast and one slow, the fast ramp does an estimate of the output voltage, while a slow ramp in the opposite direction discharge the overshoot. Another is to change the threshold of the comparator to compensate for the overshoot [54]. An overshoot can be completely cancelled if the ramp is constant.

A fundamental difference between opamp based SC and CBSC is that opamp based SC settle during charge transfer, CBSC never settle. The current from the current source is fully on until it is turned off. In an opamp based SC all currents in capacitors and switches (outside of the opamp)

go asymptotically to zero as the opamp settle. In CBSC the current in capacitors and switches are in one of two states, constant or zero, and they are only zero when the final value has been determined. As a result, switch resistance cause offset and a non-linearity (switches have signal dependent resistance) [49, 50]. But effects can be minimized by splitting the current source [50], or reducing switch resistance. Reduced current helps, but the current in CBSC is proportional to sampling frequency, so high speed require high current.

The noise properties of comparator-based and zero-crossing-based converters has been exhaustively covered by [56] and [57] and will not be discussed in this work.

A analytical model of the MDAC output voltage is presented in the next section.

10.3.1 Model of MDAC output voltage

Assume finite resistance in current source. Kirchhoff's current law give the differential equation

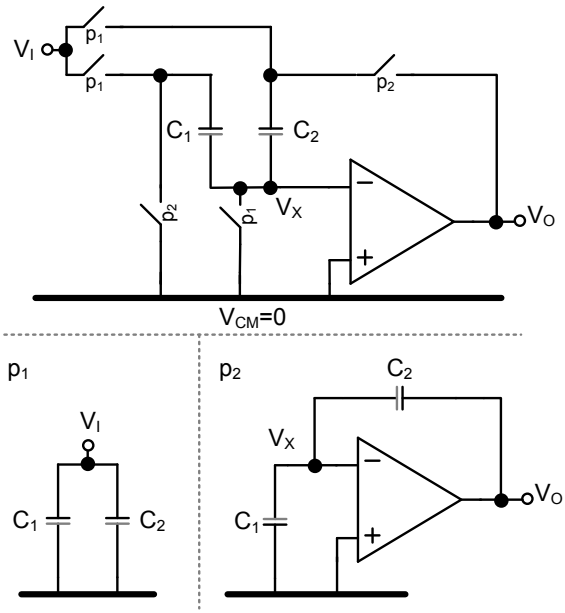
$$I_0 = C_o \frac{dV_o(t)}{dt} + V_o(t)/R_o \tag{10.3}$$

where C_o is the capacitance at the output, V_o is the output voltage, I_0 is the current in the current source and R_o is the output resistance of the current source. Solving the differential equation yields.

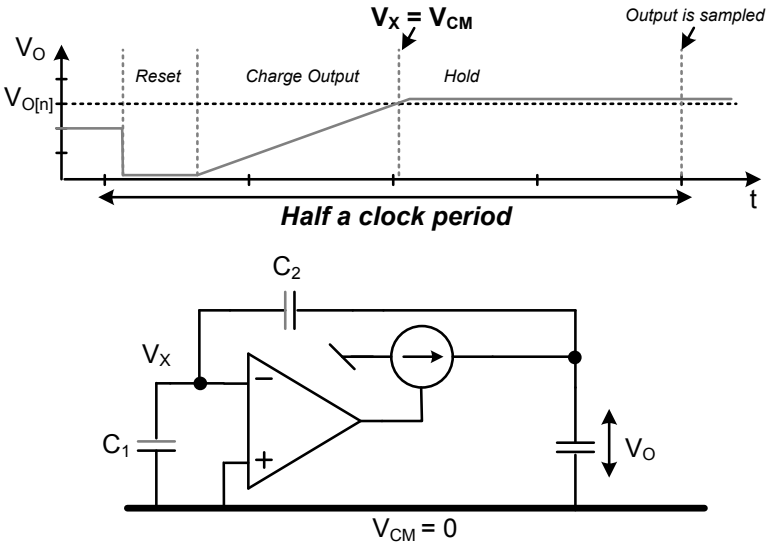
$$V_o(t) = I_0 R_o \left(1 - e^{-\frac{t}{R_o C_o}} \right) \tag{10.4}$$

The time t is the sum of T_{V_I} — the time to charge to the ideal output voltage ($V_o(t) = 2V_I$)— and the comparator delay T_d. The ideal charge time T_{V_I} is given by

$$T_{V_I} = -ln \left(\frac{-2V_I}{R_o I_0} + 1 \right) C_o R_o \tag{10.5}$$



(a) Switched-capacitor amplifier using an operational amplifier.



(b) Comparator-based switched-capacitor circuit.

Fig. 10.1: Opamp based switched-capacitor versus comparator-based switched-capacitor.

To compensate for the comparator delay the comparator threshold (V_{ct}) can be changed so the comparator start switching before $V_o = 2V_I$ is reached. Accordingly, the charge time can be written as

$$t = -ln\left(-2\frac{V_I - V_{ct}}{R_o I_0} + 1\right) C_o R_o + T_d \tag{10.6}$$

Inserting (10.6) in (10.4) results in

$$V_o(t) = 2e^{-\frac{T_d}{R_o C_o}} V_I + I_0 R_o [1 - e^{-\frac{T_d}{R_0 C_o}} (1 + 2\frac{V_{ct}}{I_0 R_o})] \tag{10.7}$$

The gain of the amplifier should be two, but from (10.7) we see the gain is smaller than two ($2e^{-T_d/R_o C_o}$). This gain error will cause static non-linearities when a CBSC circuit is used in a pipelined ADC. The gain error is a function of the comparator delay, the output resistance and output capacitance. The last term in (10.7) is the overshoot.

10.4 Implementation

The ADC is an 8-bit differential comparator-based switched capacitor pipelined ADC. It has continuous time bootstrapped input switches and comparator-based switched-capacitor MDAC. It differs from other CBSC ADCs ([54] and [48]) by being the first fully differential CBSC ADC. A system level diagram is shown in Fig. 10.2. The ADC has seven 1.5-bit pipelined stages and a 1.5-bit flash-ADC.[1]

An on-chip non-overlapping clock generator generate the clock phases from an external clock. Reference voltages are generated off-chip. Digital error correction is performed off-chip in software for testability.

Each pipelined stage is controlled by a 22-bit calibration string, generated off-chip and written to the ADC through a serial interface. The calibration string controls the comparator threshold and current source current.

[1]The ADC was designed as a 10-bit ADC with eight 1.5-bit stages and a 2 bit flash-ADC. But measurements showed more noise than expected (the noise is dominated by the the digital IO). Accordingly, the MDAC in stage 8 was turned off and the output of the flash-ADC ignored.

The circuit implementation of blocks is detailed in the following sections.

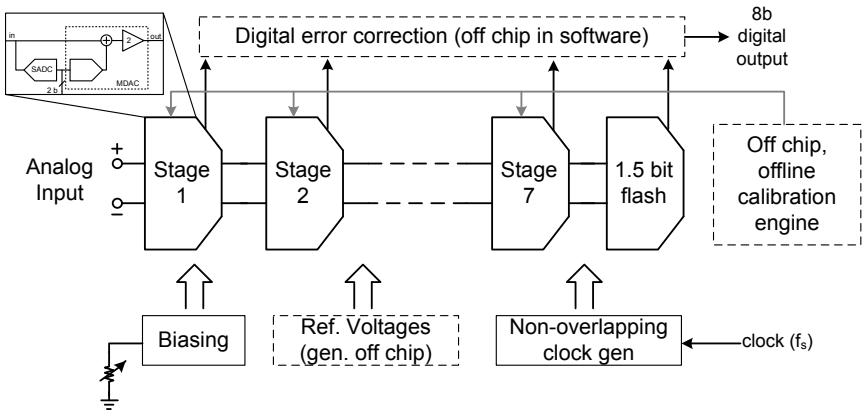


Fig. 10.2: System level diagram of pipelined ADC.

10.4.1 Sub ADC

Each stage in the pipelined ADC has a 1.5-bit analog-to-digital converter, often referred to as the sub ADC (SADC). The 1.5-bit architecture use redundancy to correct for offset errors in SADC comparators [58]. As a result, dynamic comparators can be used, which have large offsets but consume little power. In this converter the resistive divider dynamic comparator is used [35].

10.4.2 Stage MDAC architecture

Fig. 10.3 shows the MDAC of stage one and the sampling network of stage two. The stage operates on four phases p_1, p_2, p_r and p_{1a}. An advanced clock phase (p_{1a}) samples the input signal before p_1 turns off, this reduces the problem of signal dependent charge injection from p_1 switches. In phase p_1 the comparator is preset by forcing the comparator inputs to reference voltages V_{RN} and V_{RP}, so the output of the comparator is known at the end of p_1. The output is reset in p_r, forcing $V_{XP} < V_{XN}$. When p_r goes low the current sources charge the MDAC output capacitance. The comparator detects when the virtual ground condition is reached and turn off the

current sources. The input switches in the first stage are continuous time bootstrapped switches.

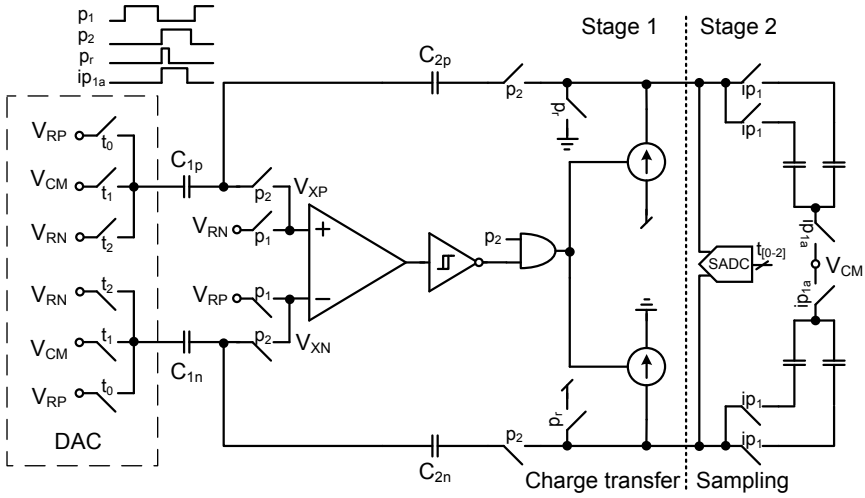


Fig. 10.3: Stage one during charge transfer and stage two during sampling.

10.4.3 Continuous time bootstrapped switch

Bootstrapped switches are used to reduce the signal dependent charge injection and signal dependent switch conductance [59]. In bootstrapped switches a constant gate-source voltage is applied to the switch. One method charges a capacitor to a fixed voltage when switch is off, and when the switch is turned on the capacitor is connected between the gate and source of the switch, thus acting as a battery to keep the gate-source voltage constant [59].

Another approach is continuous time bootstrapping [60]. A source follower tracks the input signal, the gate-source voltage of the switch is set by the gate-source voltage of the source follower. Fig. 10.4 shows the continuous time bootstrapped switch. Thick oxide transistors (marked in Fig. 10.4 by thick gates) are used to reduce reliability concerns.

The source follower M_2 is biased by M_1. An inverter (M_3 and M_4) control the gate voltage of the switch (M_S), the inverter switches between the level shifted input (V_A) and ground. When the switch is on (p_1 high) M_5 shorts the bulk of M_S to the input, reducing the body effect and improving

reliability (keeps gate bulk constant). When the switch is off M_6 shorts the bulk to ground to avoid forward biasing the bulk-drain PN junction.

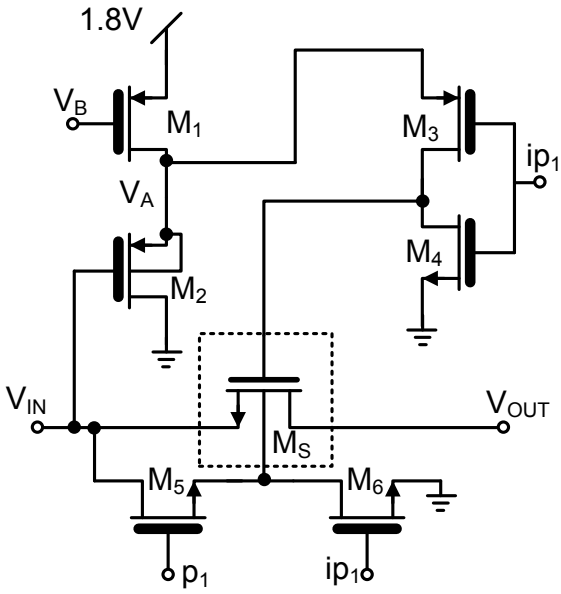


Fig. 10.4: Continuous time bootstrapped switch.

10.4.4 Comparator with adjustable threshold

A two-stage continuous time amplifier (Fig. 10.5) with a differential first stage and single ended common source second stage is used as the comparator.

In phase p_1 the comparator inputs are reset to V_{RN} and V_{RP} (as shown in Fig. 10.3), so the output is known at the end of p_1. With this preset the design of control logic between comparator and current sources is simplified. Phase p_2 start by resetting the MDAC outputs, this cause V_{XN} to increase and V_{XP} to decrease. When reset is complete the current sources start charging the MDAC outputs, as a result V_{XN} falls and V_{XP} rise.

Fig. 10.6(a), Fig. 10.6(b), and Fig. 10.6(c) shows V_{XN} and V_{XP} as a function of time for different comparator thresholds (V_{ct}). The comparator should turn off current sources when $V_{XP} = V_{XN}$, but because the compara-

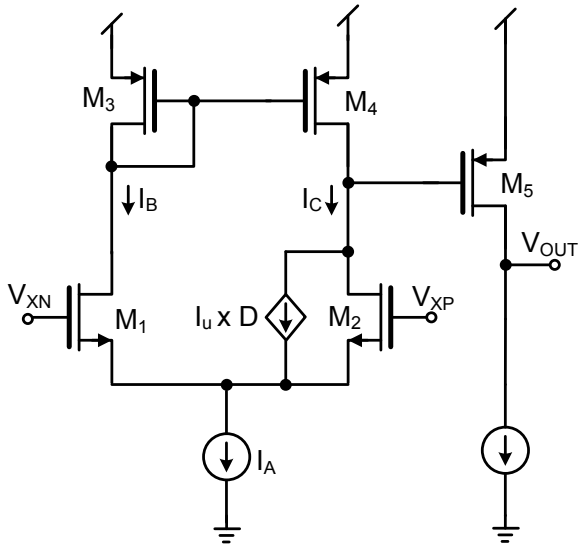


Fig. 10.5: Comparator with adjustable threshold.

tor has a delay (T_d) the current sources turn off later, causing an overshoot (Fig. 10.6(a)). Adjusting the threshold of the comparator changes the amount of overshoot. If V_{ct} is adjusted optimally there is no overshoot (Fig. 10.6(b)). If V_{ct} is lower than the optimal value the output undershoots (Fig. 10.6(c)). From the figure we see that a non-optimal threshold cause an offset in the MDAC output, as shown in (10.7). If the offset is small it is corrected by the digital error correction inherent to 1.5-bit stage architecture. Although, the extra offset from the overshoot increase the demands on the dynamic comparators because the sum of offsets must be less than $\pm V_{REF}/4$ in a 1.5-bit stage.

The comparator threshold is controlled with a 6-bit current DAC in parallel with M_2, shown as a controlled current source. In Fig. 10.5 I_u is a unit current and D is an integer given by $D = 2^0b_0 + 2^1b_1 + 2^2b_2 + 2^3b_3 + 2^4b_4 + 2^5b_5$. The current in the current source I_A is the sum of the two branch currents ($I_A = I_B + I_C$). The comparator threshold is defined as the differential input voltage when the branch currents are equal ($I_B = I_C$).

Equal currents occur when

$$\beta V_{EFF,1}^2 = \beta V_{EFF,2}^2 + I_u \times D \tag{10.8}$$

where $\beta = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}$ and $V_{EFF,X}$ is the effective gate overdrive of transistors M_X. If $D = 0$ the currents are equal when the effective gate overdrives are equal, which occurs when the positive and negative inputs are equal. If $D > 0$ the currents are equal when the effective overdrive of M_1 is larger than the effective overdrive of M_2, which occurs when $V_{IN} > V_{IP}$.

The nominal delay of the comparator (including Schmitt trigger and logic gates) is $T_d = 0.5ns$. With the 6-bit DAC the effective delay of the comparator can be controlled from $T_d = -0.9ns$ to $T_d = 0.5ns$.

10.4.5 Current sources

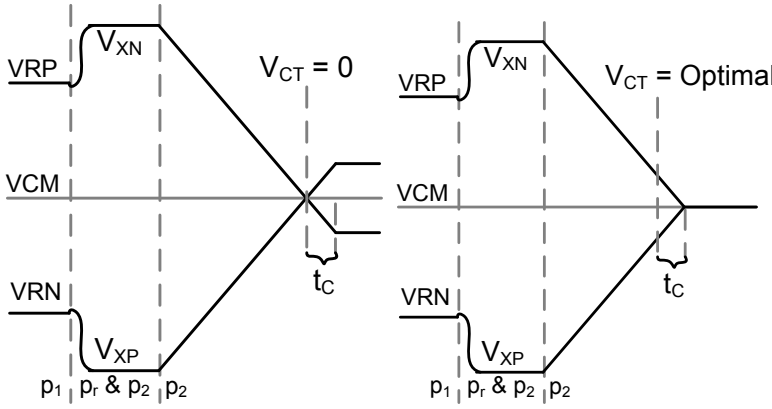
We used regulated cascode current sources to achieve high output resistance (Fig. 10.7). A PMOS current source is used for the pull up current, and a NMOS current source is used for the pull down current. Both the cascode and the common source transistors are turned off when the current source is turned off.

A single boost amplifier is shared between current sources to save power (as shown in Fig. 10.7). The amplifier sees a variable capacitive load (the load varies with how many current sources are enabled), which affects settling and stability, both manageable challenges.

The current source is programmed with an 8-bit word, with 6-bit resolution due to intentional overlap. The NMOS and PMOS sources are controlled separately. If the PMOS and NMOS currents are different the output common mode of the MDAC will be different from $(VDD-VSS)/2$. Simulations suggest that common mode feedback circuit is unnecessary.

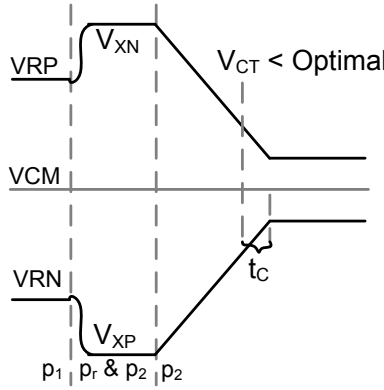
10.4.6 Bias circuits, digital error correction and reference voltages

The pipelined core has a simple bias circuit with two external bias currents. One bias current is copied to all analog blocks and the other bias current



(a) Comparator threshold equal to zero

(b) Optimal comparator threshold



(c) Comparator threshold less than the optimal value

Fig. 10.6: Voltage versus time for the nodes V_{XN} and V_{XP} as a function of comparator threshold.

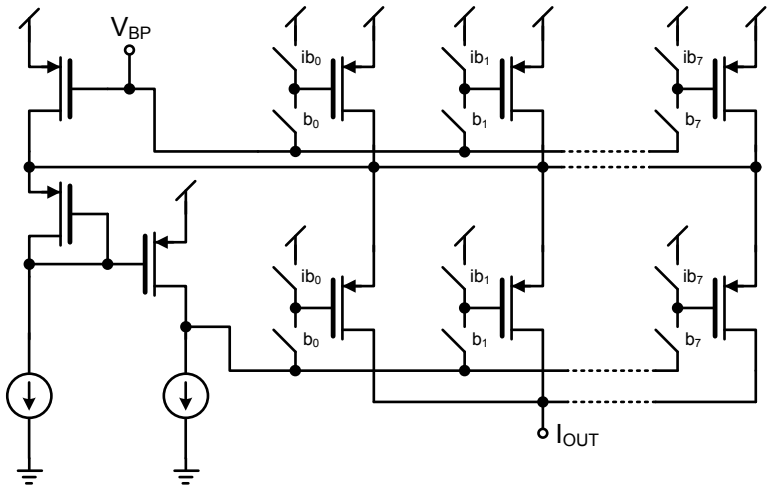


Fig. 10.7: Programmable regulated cascode current source with high output resistance.

control the delay of current starved inverters used to generate the reset phase (p_r). Current mirrors are cascoded when possible. External reference voltages are used for testability, so the power consumed by the references is not included in reported power dissipation. The digital outputs from the SADCs are brought off-chip by CMOS logic IO buffers. Synchronization, recombination and digital error correction of the output bits is performed in software.

10.5 Calibration

In CBSC some form of auto-zeroing or calibration is required. This can be seen from (10.7), the overshoot is proportional to I_0 and inversely proportional to the output capacitance of the MDAC. Both current and capacitance change with process corner.

Each stage has three calibration words, one for each current source and one for the comparator. The calibration word for the current sources is 8-bit, and 6-bit for the comparator threshold, in total, 22-bits per stage. All seven stages are calibrated, which results in $2^{154} - 1$ combinations, a large solution space.

It is impossible to test all combinations in such a large solution space.[2] So we use two different calibration algorithms: one deterministic time comparator threshold calibration, and a non-deterministic time genetic algorithm. The first algorithm calibrate the comparator delay to correct for the overshoot, while the second algorithm also calibrate the current in the current sources.

10.5.1 Deterministic time comparator threshold calibration

A flowchart of the calibration algorithm is shown in Fig. 10.8. The current source word $W_{I[N]}$ is the same for all stages, so all stages will have the same nominal current. Initially all currents are set to zero, $W_{I[0-7]} = 0$. The comparator threshold word $W_{C[N]}$ is also set to zero for all stages ($W_{C[N]} = 0$). The maximum value of the comparator threshold is $W_{CMAX} = 2^6 - 1$, and the minimum value is $W_{MIN} = 0$. M and N are the indexes of the inner and outer loop.

Calibration starts by turning on the current in the first stage ($W_{I[0]} = W_{IDEF}$, where W_{IDEF} is a sufficient current for the speed of the ADC). The comparator threshold is set to half the distance between the maximum and minimum word given by

$$W_{C[N]} = \left\lceil \frac{W_{CMAX} + W_{CMIN}}{2} \right\rceil \tag{10.9}$$

The ADC is updated with the new calibration words — in the prototype the calibration algorithm is written in software and the calibration words are written to the ADC using a serial interface, however, the calibration algorithm can easily be integrated in hardware.

The mean value of the output is calculated using a window length of L. The run time is proportional to window length, and the window length set the accuracy of the mean. We assume the input signal is a zero mean sinusoid close to Nyquist, so a window length of $L = 2^B$ is sufficient. The sign of the calculated mean plus a reference offset x_{REF} is evaluated. If it

[2] Assuming one combination could be tested each clock cycle it would take 48×10^{30} years to test all combinations

is positive the comparator threshold is increased ($W_{CMIN} = W_{C[N]}$). If it is negative the comparator threshold is reduced ($W_{CMAX} = W_{C[N]}$). The inner loop index is updated ($M = M + 1$), and the search continues. The inner loop performs a binary search for the correct comparator threshold in each stage. The outer loop turns on more and more stages as the inner loop completes.

If we assume the time spent writing the calibration words to the ADC is insignificant the calibration algorithm will complete after $7 \times 7 \times 256 = 12.5k$ clock cycles. A genetic algorithm was used to verify that this calibration algorithm finds a solution close to optimum.

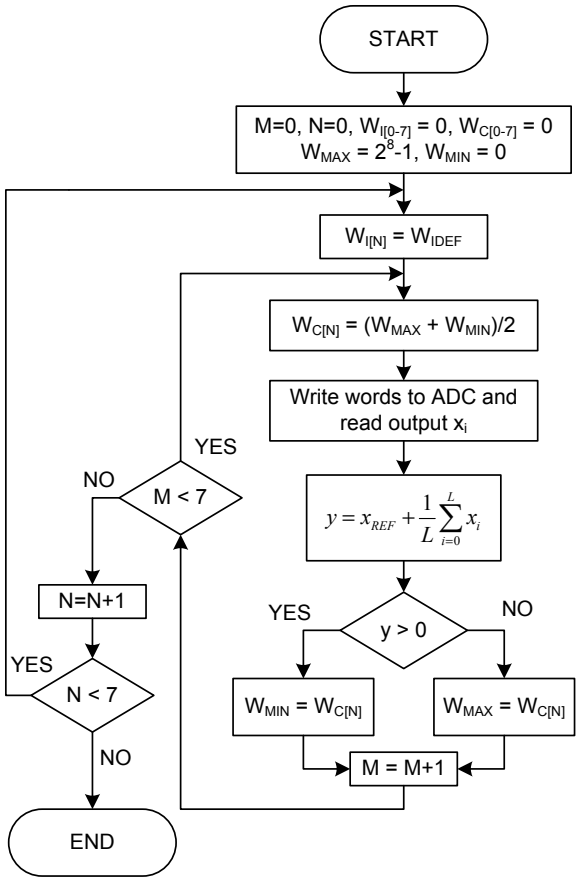


Fig. 10.8: Deterministic time comparator threshold calibration.

10.5.2 Non-deterministic calibration

To verify the comparator threshold calibration a genetic algorithm is used. A genetic algorithm models evolution and has been shown to find solutions for large search spaces [61]. The disadvantage of the genetic algorithm is the non-deterministic run time, since it cannot be determined analytically how long it takes before a good solution is found. The genetic algorithm varies both current and comparator threshold in the ADC.

10.6 Experimental results

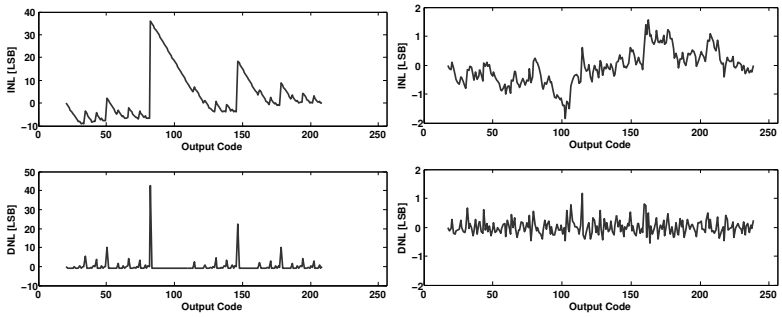
10.6.1 Results of calibration

The input signal during calibration is a sinusoidal input close to the Nyquist frequency ($f_i = 29.4MHz$). Fig. 10.9(a), Fig. 10.9(b) and Fig. 10.9(c) shows the measured *integral non-linearity* (INL) and *differential non-linearity* (DNL) for three different cases. Fig. 10.9(a) shows the INL and DNL for the default calibration words set before production based on simulation. Here the comparator threshold is too low, which results in an overshoot. For the un-calibrated case the ENOB is 2.4-bits.

Using deterministic time comparator threshold calibration the INL and DNL improves from +36/-9 LSB to +1.6/-1.8 LSB, as shown in Fig. 10.9(b). With comparator threshold calibration the ENOB is 6.5-bit. The INL shows signs of a gain error, and multiplying the bits from the first stage by 1.022 improve the ENOB to 6.9-bit. From (10.7) this suggest that either the comparator delay is too long, the output resistance is to low or capacitance is to low.

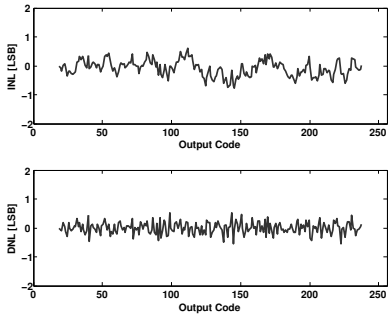
Using the genetic algorithm a better solution is found, shown in Fig. 10.9(c). The best solution improve the ENOB by 0.5-bit, resulting in a peak ENOB of 7.05-bit. This solution use less current in the first stage than used with comparator threshold calibration, which does increase the output resistance of the current sources in the first stage. According to (10.7) this would reduce the gain error, but reduced output resistance has not been confirmed as the cause of the gain error.

The best solution is used for the remainder of the measurements.



(a) No calibration, default values set before before production.

(b) Deterministic calibration of comparator thresholds with current fixed.



(c) Non-deterministic calibration of positive and negative current, and comparator threshold using a genetic algorithm.

Fig. 10.9: INL and DNL for uncalibrated, offset calibration and genetic algorithm

10.6.2 Measured power and accuracy

A summary of the ADC performance is shown in Table 10.1. It achieves a *signal-to-noise and distortion ratio* (SNDR) of 44.2-dB (7.05-bit) at Nyquist, with a sampling frequency of 60MS/s and a power dissipation of 8.5mW (5.9mW for ADC core, 2.3mW for clock generation and distribution, and 0.3mW for input switches), which result in a Walden figure of merit of 1.07

pJ/step[3] and a Thermal figure of merit of 8.09fJ/step.[4] An input signal amplitude of -1 dBFS is used. The micrograph of the ADC is shown in Fig. 10.10(c).

The ADC has a *spurious free dynamic range* (SFDR) of 60-dB close to Nyquist. The SNDR and SNR change little with input frequency, and the effective resolution bandwidth extend well beyond the Nyquist frequency (Fig 10.10(b)). The SFDR change with frequency and is maximum close to Nyquist. The calibration algorithm used this frequency and we assume that is why the SFDR best at that frequency.

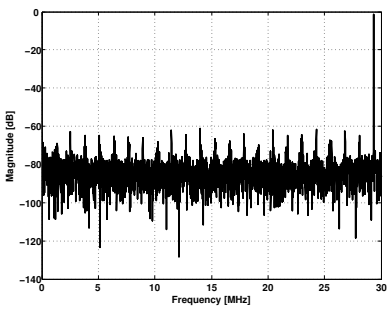
A 8192 point FFT of the ADC output is shown in Fig 10.10(a). Coherent sampling and a Hanning window is used to avoid spectral leakage of the fundamental.

Simulation of the ADC showed a peak SNDR of 9-bits (the ADC was designed as a 10-bit ADC), but as [50], we measured more noise than expected. Most of the extra noise appear to be coming from digital IO. As [50] we noted a strong correlation between digital IO supply voltage and noise level in the ADC. In theory the power supply rejection is better in a differential design, which could suggest that there is mismatch between the differential paths in the ADC, but this has not been quantified. As a result of the noise from digital IO, the IO used a voltage supply of 0.84V, which limited the speed of the converter to 60MS/s. Increased speed can be achieved, but only by increasing the digital IO supply voltage, which in turn increase the noise (5.5-bit ENOB at 1.2V digital IO supply voltage).

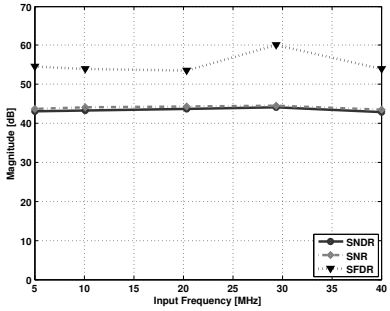
10.7 Conclusion

The first differential comparator-based switch capacitor (CBSC) pipelined ADC was presented. The switched-capacitor multiplying digital-to-analog converter (MDAC) use current sources and a comparator to do charge transfer. Continuous time bootstrapped switches were used in the first stage to reduce signal dependent switch resistance. A simple calibration algorithm

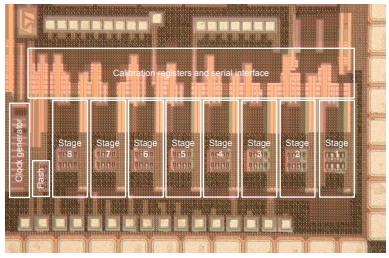
[3] $FOM = P/2^B f_s$
[4] $FOM = P/2^{2B} f_s$



(a) A 8192 point FFT of the ADC output.



(b) SNDR, SNR and SFDR versus frequency, sampling frequency is 60MS/s. Calibration words are constant.



(c) Chip micrograph. Stage 8 and flash-ADC are not used.

Fig. 10.10: FFT of ADC output, dynamic parameters versus frequency, and chip micrograph.

Table 10.1: Summary of calibrated ADC performance

Technology	1.2V/1.8V 90nm CMOS
Sampling Frequency	60 MS/s
Resolution	8 bits
Full scale input	0.8V
Size	0.85mm x0.35 mm
DNL (LSB)	0.52 / -0.54
INL (LSB)	0.6 / -0.77
SNR (29.4MHz input)	44.5 dB
SNDR (29.4MHz input)	44.2 dB
SFDR (29.4MHz input)	60 dB
ADC core power	5.9mW
Clock power	2.3mW
Input switches (1.8V)	0.3mW
Waldon Figure of Merit	1.07 pJ/step
Thermal Figure of Merit	8.09 fJ/step

correct for comparator delay variation due to manufacturing. Calibration reduce ramp overshoot, which dominate the non-linearity in CBSC ADCs. The ADC was produced in a 90nm low-power CMOS technology. The ADC core is 0.85mm x 0.35mm, with a 1.2V supply for the core and 1.8V for input switches. The ADC has an effective number of bits (ENOB) of 7.05-bit, and a power dissipation of 8.5mW at 60MS/s.

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Chapter 11

Comments to papers, conclusion and further work

11.1 Comments to papers

11.1.1 Paper 2

In the suggested future work of this paper we mention that an integrated circuit implementation would be the next step. We did investigate some implementations on the simulation level, but we discovered that low-pass noise shaping was insufficient to create an efficient high-speed, high-resolution ADC. With a high oversampling ratio in a high-speed modulator the requirements for the unity gain of the opamps was to high. Thus, we decided to concentrate on more aggressive noise shaping using zeros at non-zero frequency to lower the OSR of the modulator.

11.1.2 Paper 4

The comparator developed in this paper was intended for the pipelined ADCs in this thesis (Paper 5 and Paper 7), but a problem was discovered after publication. The comparator in Paper 4 has significant kick-back through the input transistors M1 and M4. In the reset phase the drain of these transistors are reset to ground. When the comparator turns on, both

the sources go to VDD. This results in a kick-back through the gate-source capacitor. The kick-back can become large if input capacitance of the comparator is significant compared to the sampling capacitors in the pipelined stage. As a consequence, this comparator was not used in Papers 5 and Paper 7.

11.1.3 Paper 7

Fig. 11.1 shows a comparison of this ADC to other 8-bit converters. At 8-bits and above 1MS/s there are three converters that have better FOM. The first is a zero-based crossing switched-capacitor (similar to CBSC) by Brooks et al with 4.5fJ/step at 200MS/s [50], this was a single ended architecture implemented in 0.18μm CMOS. The second is by Kim et al [62] in a 0.18μm CMOS technology with a FOM of 3.56fJ/step at 200MS/s. They used switched-opamps to reduce power dissipation. The third is by Mulder et al [63] with 4.5fJ/step at 125MS/s, this was a sub-ranging ADC in 0.13μm CMOS technology. At 8-bit and above 1MS/s there is only one other ADC in 90nm CMOS by Shen et al [64], which has a FOM of 11.37fJ/step at 10MS/s.

The ADC in Paper 7 was designed to be a 10-bit converter, but we underestimated the noise from digital IO, which limited the performance. Thus, the ADC was not optimized for 8-bit operation, and in that light the achieved performance is satisfactory.

11.2 Conclusion

In this thesis we have focused on two of the challenges facing an ADC designer in nano-scale CMOS technology, reduced power supply and reduced output resistance.

For high-resolution ($\geq$ 12-bit) ADCs one of the challenges is the increased capacitance due to reduced signal swing. As seen in Fig. 1.1 the power supply is expected to reach 0.65V at the 14nm node (year 2020). If we assume the signal swing is 80% of the power supply a 12-bit ADC will require a minimum of 12pF sampling capacitance, while a 14-bit ADC will

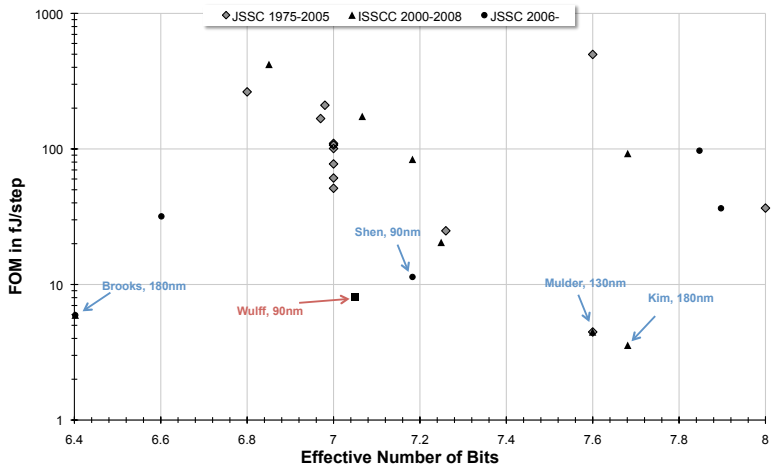

Fig. 11.1: Figure of merit comparison of the ADC in Paper 7 and other eight bit converters with sampling frequency above 1MS/s. A lower value is better.

require 192pF sampling capacitance. Hence, high-resolution converters in nano-scale CMOS must use oversampling to reduce the capacitance.

The switched-capacitor open-loop sigma-delta modulator introduced in this work is a new architecture. In this thesis we have described how one can build such an ADC and explained most of the theory behind OLSDM. We believe that OLSDM is an interesting alternative to the MASH[1] sigma-delta as a front-end to pipelined ADCs.

Another challenge for pipelined ADCs and sigma-delta ADCs is reduced headroom and reduced output resistance. The reduced headroom makes it harder to stack transistors (cascoding) to achieve high gain. This combined with the reduced output resistance of nano-scale CMOS transistors make it difficult to design high gain circuits. Unless something is done at the device level it will be challenging to design high gain ($>$ 40dB) operational amplifiers in the future nano-scale CMOS technologies.

For high-resolution ($\geq$ 12-bit) high-speed ADCs techniques like correlated-level shifting [46] or gain-calibration [53] could be alternatives to conventional opamps.

[1]MASH: Multi-stAge noise SHaping

For low- to medium-resolution (6-bit to 10-bit) high-speed ADCs techniques like open-loop residue amplifiers and comparator-based switched-capacitor circuits are an alternative to opamp-based SC.

For pipelined ADCs up to 7-bit the open-loop residue amplifier is a good option, as was demonstrated in Paper 5. But the use of open-loop residue amplifiers above 7-bit requires calibration due to the non-linearity of open-loop amplifiers.

Comparator-based switched-capacitor ADCs can bridge the gap from 7-bit to 10-bit resolution. We have shown that it is possible to create a differential CBSC ADC. And we have shown that the efficiency of such a converter is good. The ADC in Paper 7 is only two times less efficient than the best 8-bit ADCs above 1MS/s. To par the best ADCs it would have to increase its resolution by 0.5-bit (from 7.05-bit to 7.5-bit). As the pipelined ADC in Paper 7 was designed for 10-bit operation and achieved 9-bit ENOB in simulation we believe that differential CBSC pipelined ADCs can be made more efficient than our prototype. The limiting factor in our ADC was noise from digital IO, which is an problem that can be solved.

11.3 Further work

For open-loop sigma-delta modulation the next question is: What is the expression for the effect of incomplete settling in the modulo resonator and the modulo integrator? The effects of incomplete settling are well known for conventional integrators, but it must be verified that the modulo operation does not introduce any new phenomena. An analytical expression that can be translated into a MATLAB model is needed, and it should be verified with SPICE simulations. A place to start is with the papers by Temes [26] and Martin [27], which detail the effects of incomplete settling for switched-capacitor integrators.

For comparator-based switched capacitor ADCs there are two challenges we would like to mention. Our ADC has digitally controlled current sources and comparators and a digital calibration algorithm is used to calibrate the ADC. But the search space is too large, $2^{154} - 1$ is simply too many possible

solutions. In future versions we would recommend limiting the search space. One way to do this is to reduce the number of CBSC stages. We believe that a combination of MSB CBSC stages and LSB opamp-based stages, LSB open-loop residue amplifier stages, or a multi-bit flash-ADC is the way to go. For example a 10-bit pipelined ADC with four CBSC stages and a 6-bit back-end. The search space for calibration of CBSC stages is then reduced. With our calibration method there would be $2^{88}-1$ possible solution, which still is too many. But with the help of the design equations in Paper 6 the search space can be further reduced. The necessary comparator threshold (V_{ct}) can be calculated from the comparator delay (T_d), the current source current (I_0), the output capacitance (C_o) and the output resistance (R_o). With SPICE simulations the standard deviation of these variables can be found. Accordingly, the standard deviation of V_{ct} could be found, which would limit the number of bits required to calibrate it after production.

Another challenge is the noise from digital IO. For future prototypes we would recommend synchronizing all bits. Knowing when the digital outputs switch is essential. Reducing the number of bits would also be a good idea. For a pipelined ADC with four CBSC stages and a 6-bit back-end we would need $2 \times 4 + 6 = 14$ digital outputs, compared to 18 digital outputs for eight CBSC stages and a two bit flash-ADC. In addition, in an ADC prototype is a good idea to include a down-sampler, so the digital outputs can be run at a lower speed than the ADC core. We did not do this for the ADC in Paper 7, but we wish we had.

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