Bootstrapped Switch In Low-Voltage Digital 90nm CMOS Technology

Christian Lillebrekke, Carsten Wulff and Trond Ytterdal

Department of Electronics and Telecommunication, Norwegian University of Science and Technology,
N-7491 Trondheim, Norway

***Abstract*— The design of a bootstrapped switch in digital 90 nm CMOS technology, with 1.0 V supply voltage and 1 GHz sampling frequency for a 300 fF capacitive load is presented. Simulation results indicate that the switch has 10 bit linearity up to an input signal of 1.0 V peak-to-peak and frequency of 100MHz. The switch is intended for use in state-of-the-art data converters.**

I. Introduction

To follow the trend of Moore's law it has been necessary to scale down, not only geometries, but also voltages and currents used in circuitry. Operating at lower voltages always leads to new problems and challenges in the design of analog circuits. [1]

The need for low power circuits was in earlier generations limited to special niche products, such as pace-makers, watches and hearing aids. Low power consumption was close to the last item on the list of specifications for VLSI engineers. As portable electronics, such as lap-tops and cellular phones, have become widespread in daily life this situation has changed drastically.

Low supply voltage can be a requirement resulting from the system or process or as a result from a power reduction strategy in digital circuitry. Although reduction in supply voltage can be an effective method for reducing power consumption in digital circuits, this has little influence in analog circuits. Lower signal amplitudes require lower noise floor and complicates the design of analog circuits [1].

High performance analog circuits often employ Switched-capacitor (SC) circuits. Analog switches which can conduct reliably in the rail-to-rail range is often difficult to design in low voltage circuits. This paper describes a simple, yet efficient, switch for reliable rail-to-rail operation in a state-of-the-art, low-voltage digital 90 nm CMOS technology.

II. Analog Switches

In SC circuit design, opamps, capacitors and switches are the most important building blocks. An ideal switch has infinite off-resistance and zero on-resistance. A MOSFET transistor can be used to implement a switch, source and drain act as the switch terminals and the gate (and bulk) can be used to control the conductivity.

A drawback with such an implementation is that the conductivity of the channel between the two terminals, is strongly dependent on the potentials of the terminals, relative to the channel potential. The resistance in a conducting transistor in linear region is expressed in the slightly simplified equation (1) [2].

$$R_{ON} \approx \frac{1}{g_{ds}} = \frac{1}{\mu * C_{ox} \frac{W}{L} (V_{gs} - V_{th})} \tag{1}$$

where V_{gs} the gate-source voltage, μ electron mobility, C_{OX} the oxide capacitance, W and L width and length of the transistor and V_{th} the threshold voltage. This equation is only valid when V_{gs} is equal to or bigger than V_{th}. If the gate-source voltage decrease beyond V_{th} the resistance increase abruptly.

III. Bootstrapped Switch

Bootstrapped switches is a circuit technique to alleviate the problem with poor conduction and varying on-resistance. These switches are in principle realized with a single pass transistor and additional devices for generation of gate-source voltages for the pass transistor. During the off-state the gate is connected to ground and the transistor cutoff. The big difference from regular analog switches is present in the on-state, where the gate to channel voltage is kept constant. This is done by connecting a constant offset voltage between the gate and source terminals of the main switch. This voltage can be obtained by the use of a capacitor pre-charged in the off-state. Depending on the input signal, this offset can reach voltages equal to V_{dd}. Since the absolute voltage at the gate terminal exceeds the supply voltage, these switches have to be designed carefully so that they don't violate any reliability constraints. Several topologies can be found in the open literature, such as [3], [4] and [5]. The latter also compensates for the unwanted body-effect.

IV. Circuit Design

The proposed circuit is based on the topology presented in [6] and shown in figure 1. This illustration shows the basic bootstrap technique and consists of a main switch (SW), five additional switches and a bootstrap capacitor. The circuit is controlled by two non-overlapping clock signals. During the off-phase (phi2) C_{boot} is pre-charged through switches S3 and S4, while S5 connects the gate of SW to ground. During the on-state S1 and S2 connects the capacitor to the gate and

source terminals of SW. This connection makes V_{gs} equal to V_{dd} plus the input voltage during the on-phase. (phi1)

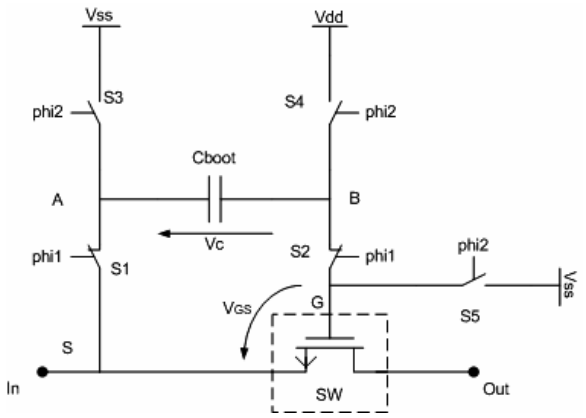

Fig. 1. The implemented topology.

The transistor level implementation of the switch is shown in figure 2. This implementation originates from the basic circuit. The topology is similar to the circuit in [6], except from the dummy transistor at node E. Transistors N1, P2, N3, P4 and N5 represents the five ideal switches. Transistor sizes were chosen to meet given specifications without violating reliability constraints. Sizing was based on the given load capacitance of 300 fF and the minimum transistor length of 0.1 μm. The dummy switch (PD) is used to reduce the effect of charge injection at node E.

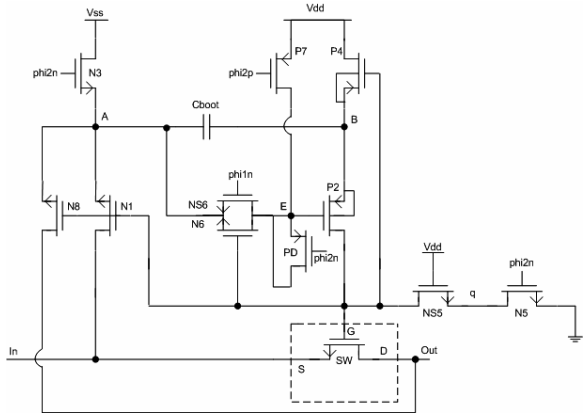

Fig. 2. Transistor implementation.

The switching operation is controlled by an external clock generator producing the non-overlapping clock signals shown in figure 3. The non-overlap is exaggerated in the figure for illustration purpose.

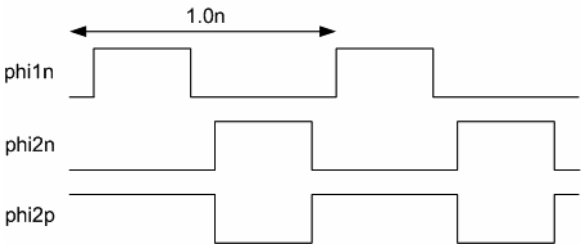

Fig. 3. Control signals for the switch.

V. Simulation Results

Simulations were performed using Mentor Graphics Eldo and a digital 90 nm CMOS process. The performance of the switch is presented in table I. Numbers are given for typical operating conditions.

TABLE I

Simulation results of the switch.

Parameter	Specification	Simulation
Capacitive load	300 fF	300 fF
Max rise/fall time	500 ps	266 ps
On-Resistance	200 Ω	75 Ω
Linearity	0.1 % THD	0.1 % THD[1]

1) *Up to 100 MHz input.*

The switch and load capacitance will form a RC circuit with a characteristic time constant. With a larger load, this constant will increase and introduce a larger delay in the output signal. In addition to the RC time constant, an internal delay in the switch will result in a hold-up before the switch turns on. The total delay for this switch, with 300 fF load, was measured to be 266 ps, which allows the desired operating frequency of 1 GHz.

On-resistance variation is normally a big source of non-linearity in switches, bootstrapped switches minimizes this variation [6]. The simulated on-resistance is shown in figure 4. It can be seen that it has a relatively small variation depending on the common-mode voltage. The figure shows results for worst- (continuous), best- (dashed) and typical (dotted) operating conditions.

The simulated total harmonic distortion (THD) at different input frequencies is shown in figure 5. The THD is below 0.1 % up to approximately 100 MHz with 1.0 V peak-to-peak. This is equivalent to 10-bit linearity and suitable for high resolution data converters.

Although this switch does not compensate for the body-effect, it proved excellent results by using a simple circuit.

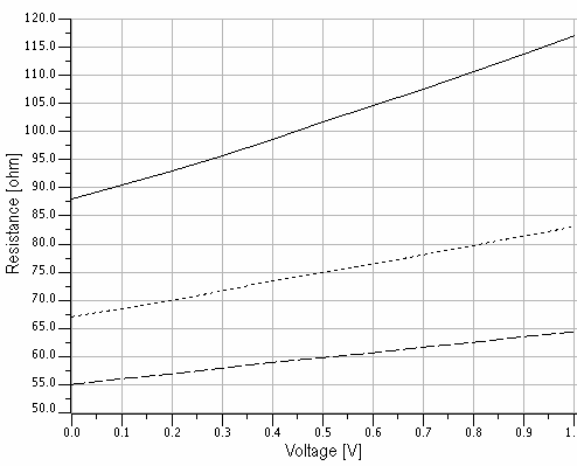

Fig. 4. On-resistance in the switch as a function of common mode voltage. Results are shown for worst- (continuous), best- (dashed) and typical (dotted) operating conditions.

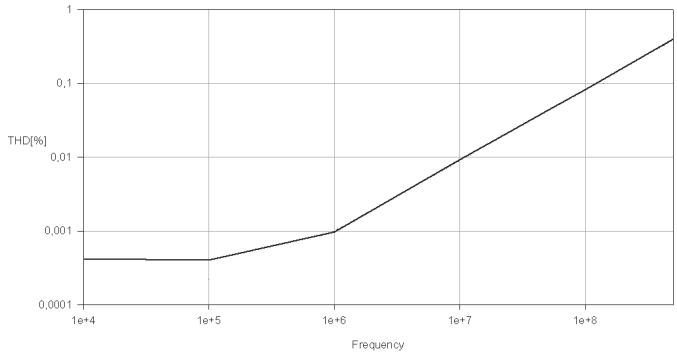

Fig. 5. Total Harmonic distortion.

VI. Future Work

This switch is prepared for implementation in a scheduled high performance data converter. A prototype is scheduled for production in the coming year. Reliability testing in a lab environment will be performed on the fabricated chip to validate simulation results.

VII. Conclusion

We have presented a bootstrapped switch scaled to fit a load of 300 fF. This switch has 1.0 V supply voltage and 1 GHz sampling frequency. In addition to circuit simplicity and speed, the circuit offers 10-bit linearity up to 100 MHz with 1 V peak-to-peak. There are to our knowledge not yet published any results of a bootstrapped switch with this performance. The symmetrical switch is ready for future implementations in low-voltage, state-of-the-art data converters in digital 90nm CMOS technology.

References

[1] E.A.Vittoz, "Low-power low-voltage limitations and prospects in analog design," *CSEM, Swiss Center for Electronics and Microtechnology*, 1994.

[2] D.A.Johns and K.Martin, *Analog Integrated Circuit Design*. John Wiley and sons, 1997.

[3] A.M.Abo and P.R.Gray, "A 1.5 V, 10-bit, 14.3-MS/s, CMOS pipeline analog-to-digital converter," *IEEE Journal of Solid-State Circuits*, 1999.

[4] J. Steensgaard, "Bootsrapped low-voltage analog switches," *IEEE Journal of Solid-State Circuits*, 1999.

[5] M.Waltari and K.Halonen, "Bootstrapped switch without bulk effect in standard CMOS technology," *Electronic letters*, 2002.

[6] M. Dessouky and A. Kaiser, "Very low-voltage digital-audio modulator with $\triangle\sum$ 88-dB dynamic range using local switch bootstrapping," *IEEE Journal of Solid-State Circuits*, 2001.