Compiling analog-to-digital converters in multiple nanoscale technologies

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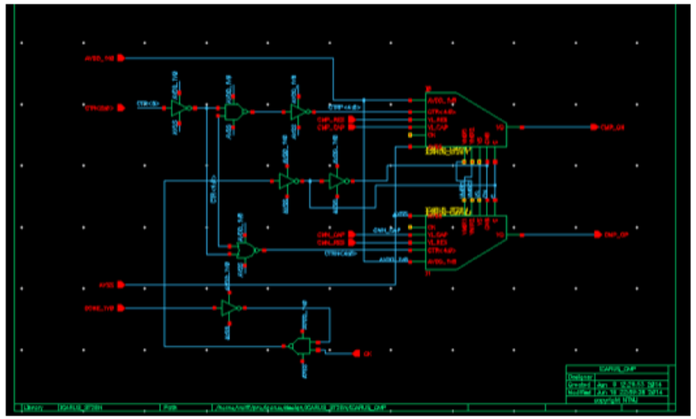
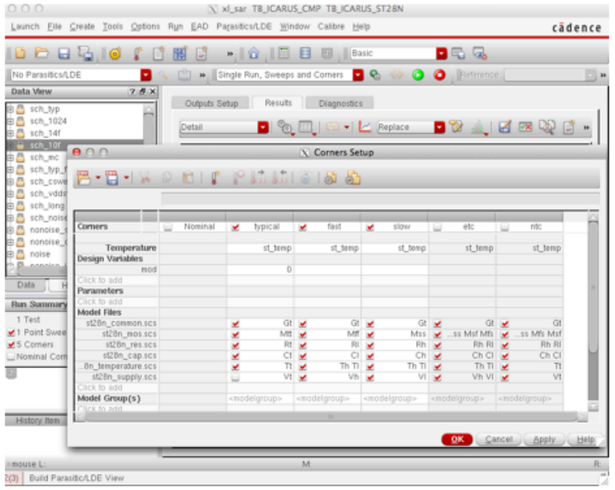
Highlights

- The day of a analog circuit designer
- Choice of specifications
- Generating physical layout
- Information needed to describe an ADC
- Compiler

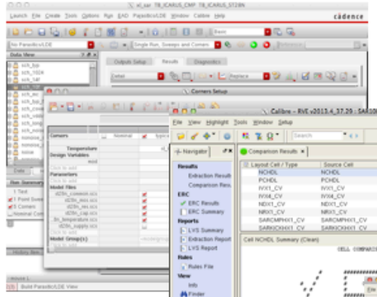
Schematic



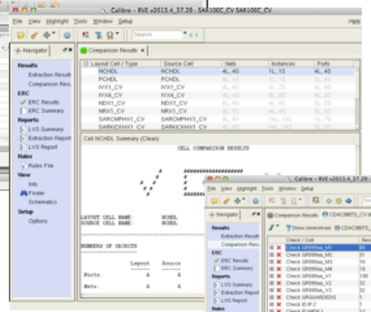
Simulation



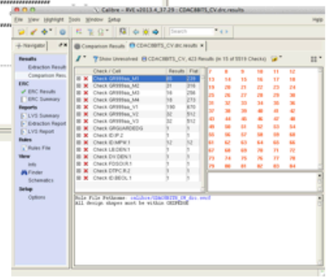
Simulation



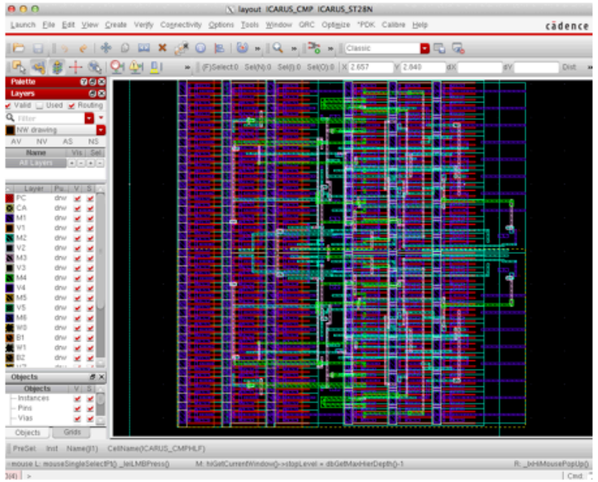
LVS

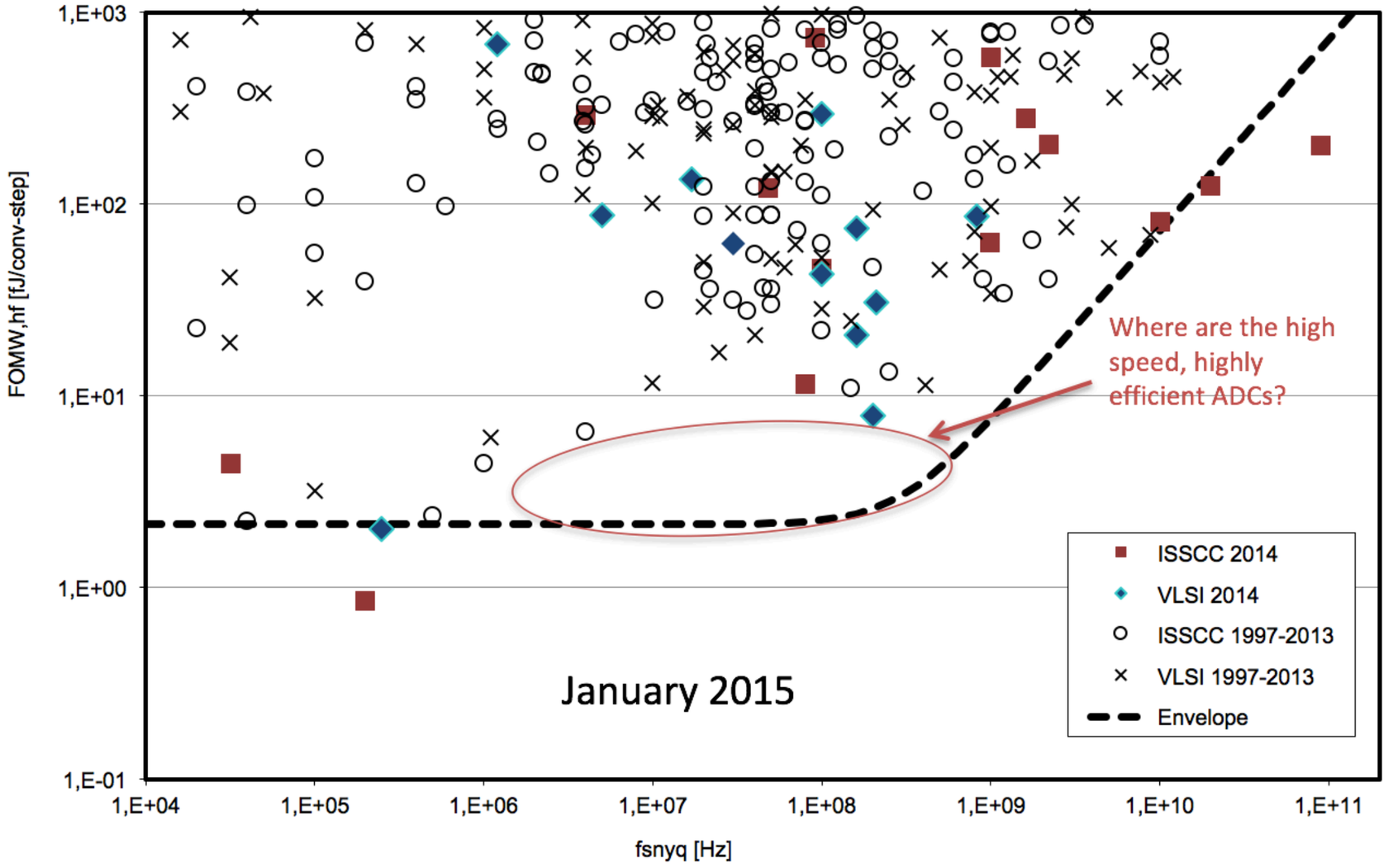


DRC



Layout

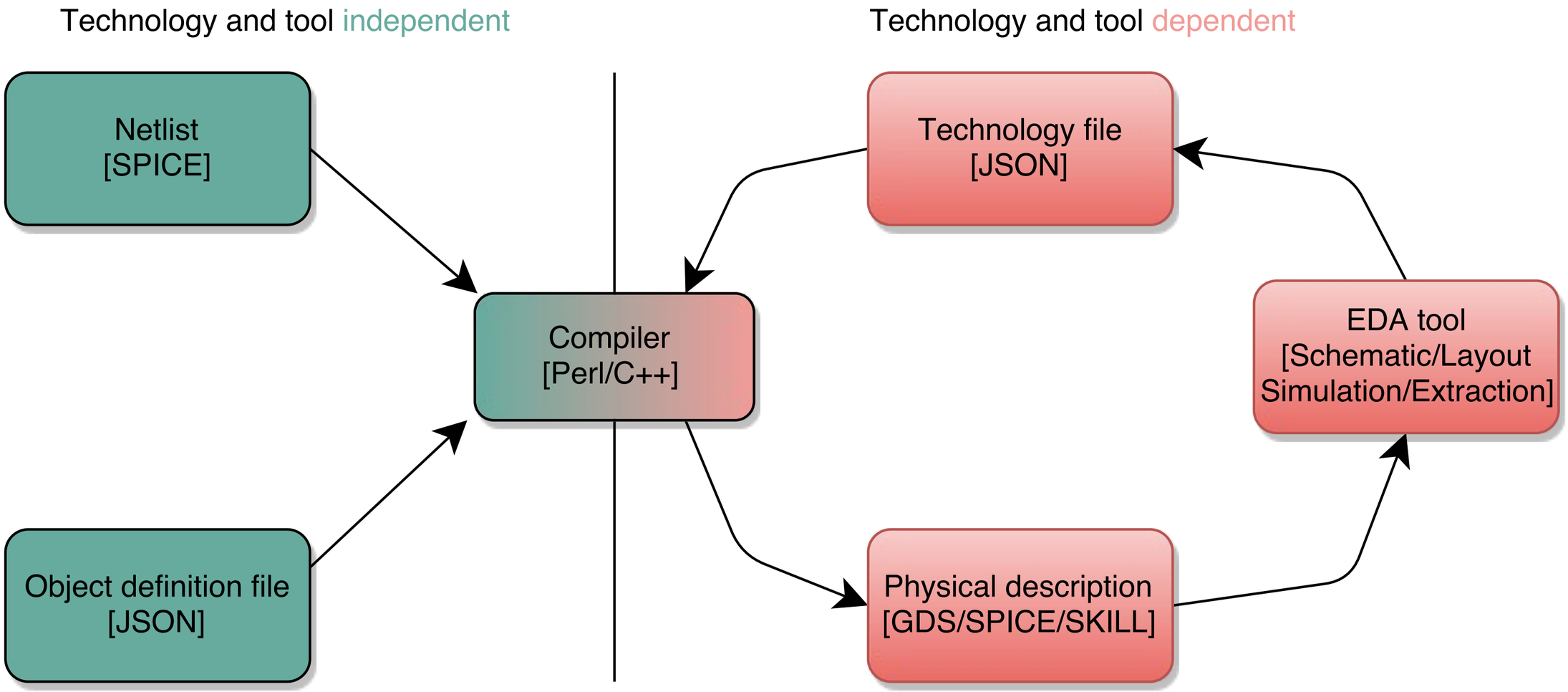




B. Murmann, "ADC Performance Survey 1997-2014," [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html.

Idea: Generate schematics and layout with a script

- cnanokit: Tool developed at Nordic to generate simple transistors, current mirrors and OTA
- cnano: Develop extension that allows generation of schematics and layout of complete ADCs
- Goal: From schematics to extracted layout in a day for a complete ADC


Technology and tool independent
Technology and tool dependent
Netlist
[SPICE]
Object definition file
[JSON]
Compiler
[Perl/C++]
Technology file
[JSON]
Physical description
[GDS/SPICE/SKILL]
EDA tool
[Schematic/Layout
Simulation/Extraction]

Netlist [SPICE]

- Connectivity described by standard netlist.
- Can be generated from any schematic tool

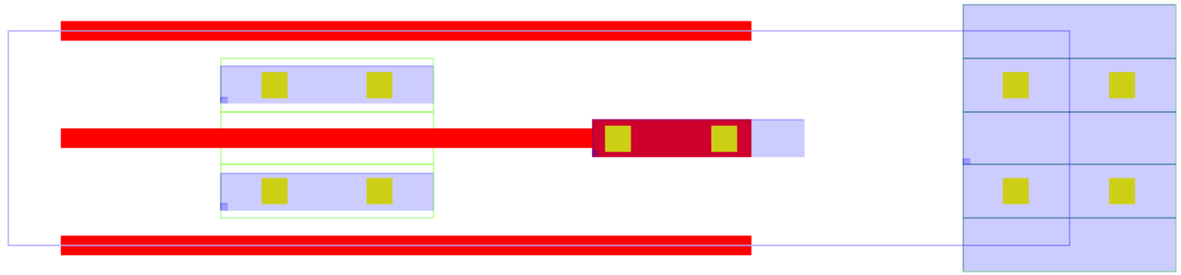
```
.subckt IVX1_CV A Y AVDD AVSS
MN0 Y A AVSS AVSS NCHDL
MP0 Y A AVDD AVSS PCHDL
.ends IVX1_CV
```

Object definition file [JSON]

- Definition of unit cells (transistors, capacitors, resistors)
- Inheritance
- Rules to route the cells
- Sequence of events (beforePlace, afterPlace, beforeRoute, afterRoute)
- Data for instructions in the compliler (addDirectedRoute, addConnectivityRoute, addPort, addVia)

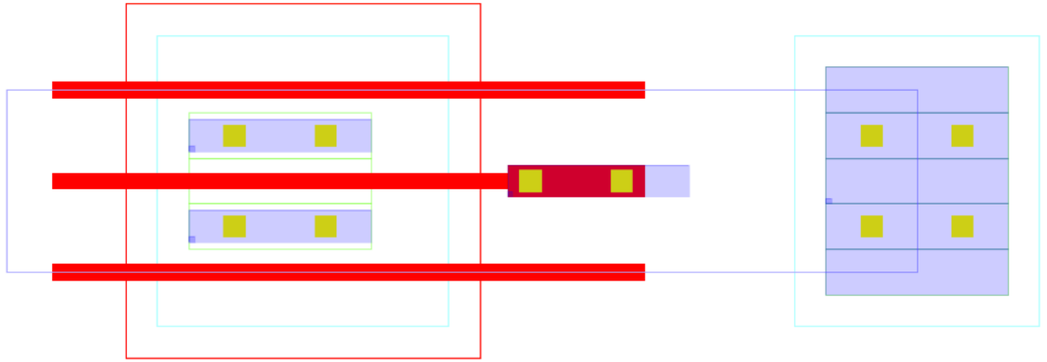
Unit cells: The transistor

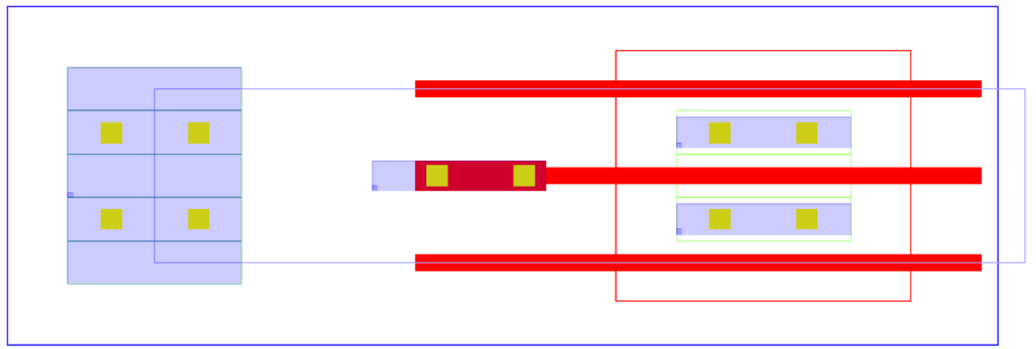
```
{ "name" : "DMOS" ,
  "fillCoordinatesFromStrings" : [
      [   "OD",
          "------------------xxxx",
          "----xxK-----------xCxC",
          "----xxx-----------xxxx",
          "----xxK-----------xCxC",
          "------------------xxxx"
      ],
      [   "PO",
          "-mmmmmmmmmmmmm--------",
          "----------------------",
          "-mmmmmmmmmmcxc--------",
          "----------------------",
          "-mmmmmmmmmmmmm--------"
      ],
      [   "M1",
          "------------------xxxx",
          "----wDww----------xxxx",
          "-----------wGww---xBxx",
          "----wSww----------xxxx",
          "------------------xxxx"
      ]
  ]
}
```



Inheritance: PMOS and NMOS

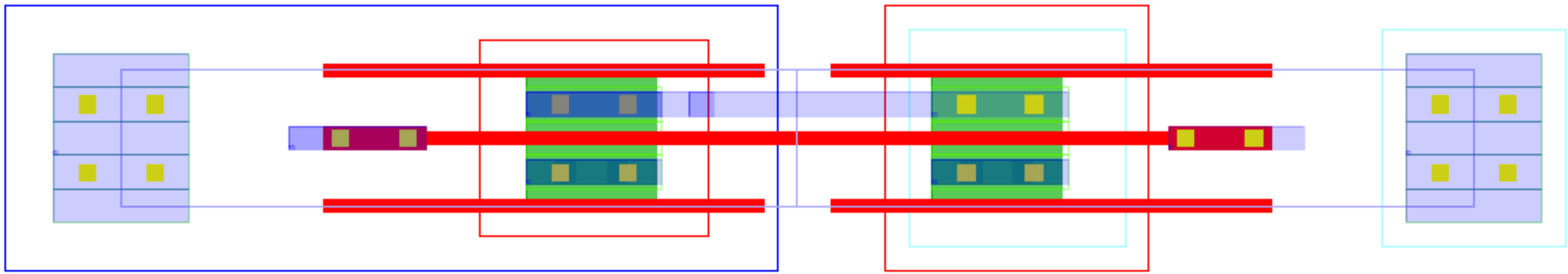
```
{ "name" : "PCHDL",
  "inherit" : "DMOS",
  "type" : "pch_lvt",
  "beforePlace" :{
     "addEnclosures" : [
       ["OD",0,["PP","NOSOI"]]
     ],
     "addEnclosuresByRectangle" : [
       ["OD",[4,0,5,5],["PP","LVT","HSSOI"]]
     ]
  }
}
{ "name" : "NCHDL",
  "inherit" : "DMOS",
  "xoffset" : -2,
  "type" : "nch_lvt",
  "afterNew" : {
     "mirrorPatternString" : 1
  },
  "beforePlace" :{
     "addEnclosures" : [
       ["OD",1,["LVT"]]
     ],
     "addEnclosuresByRectangle" : [
       ["OD",[0,0,20,5],["NW","HSSOI"]],
       ["OD",[0,0,4,5],["NOSOIN"]]
     ]
  }
}
```



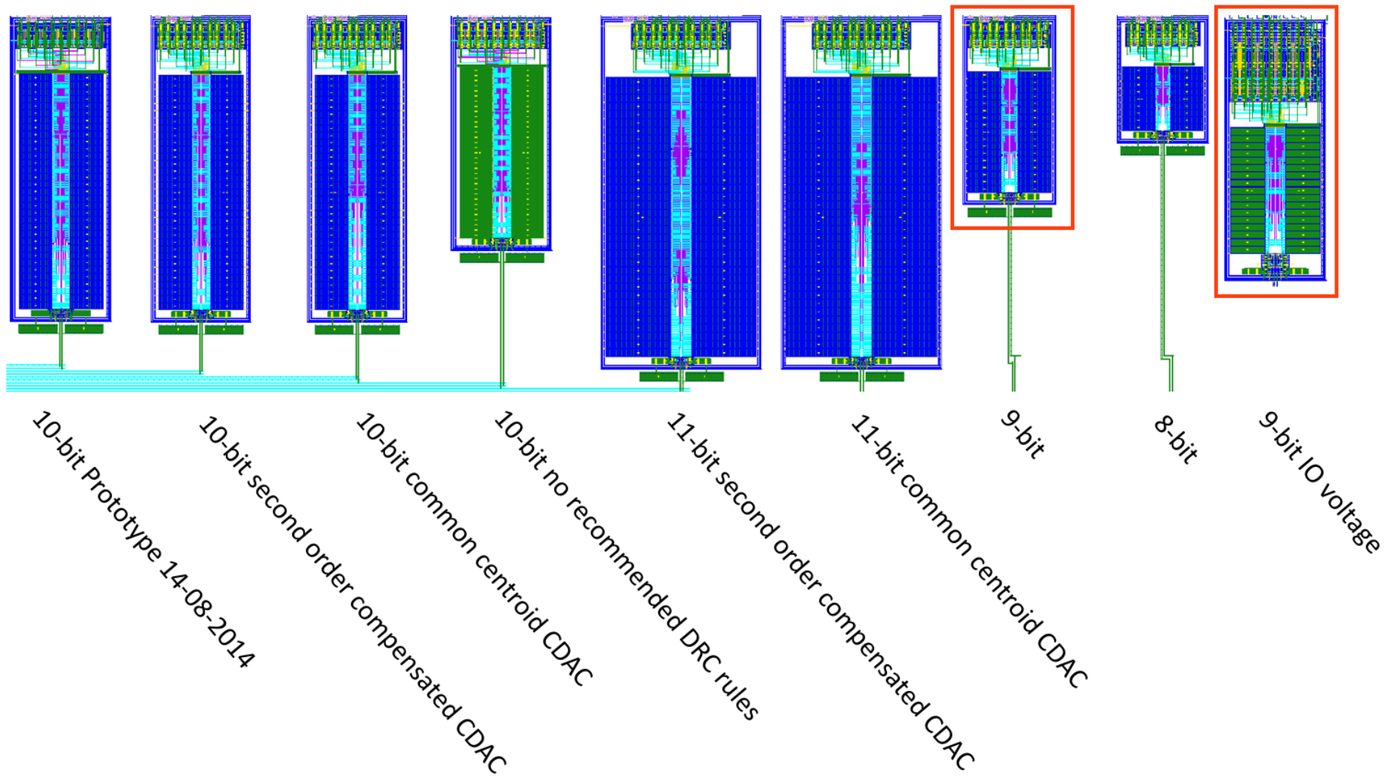


Rules to route cells

```
{ "name": "IVX1_CV" ,
  "beforeRoute" : {
    "addDirectedRoutes" : [
      ["M1","Y","MN:D-|--MP:D"],
      ["PO","A","MN:G-MP:G"]
    ]
  }
}
```

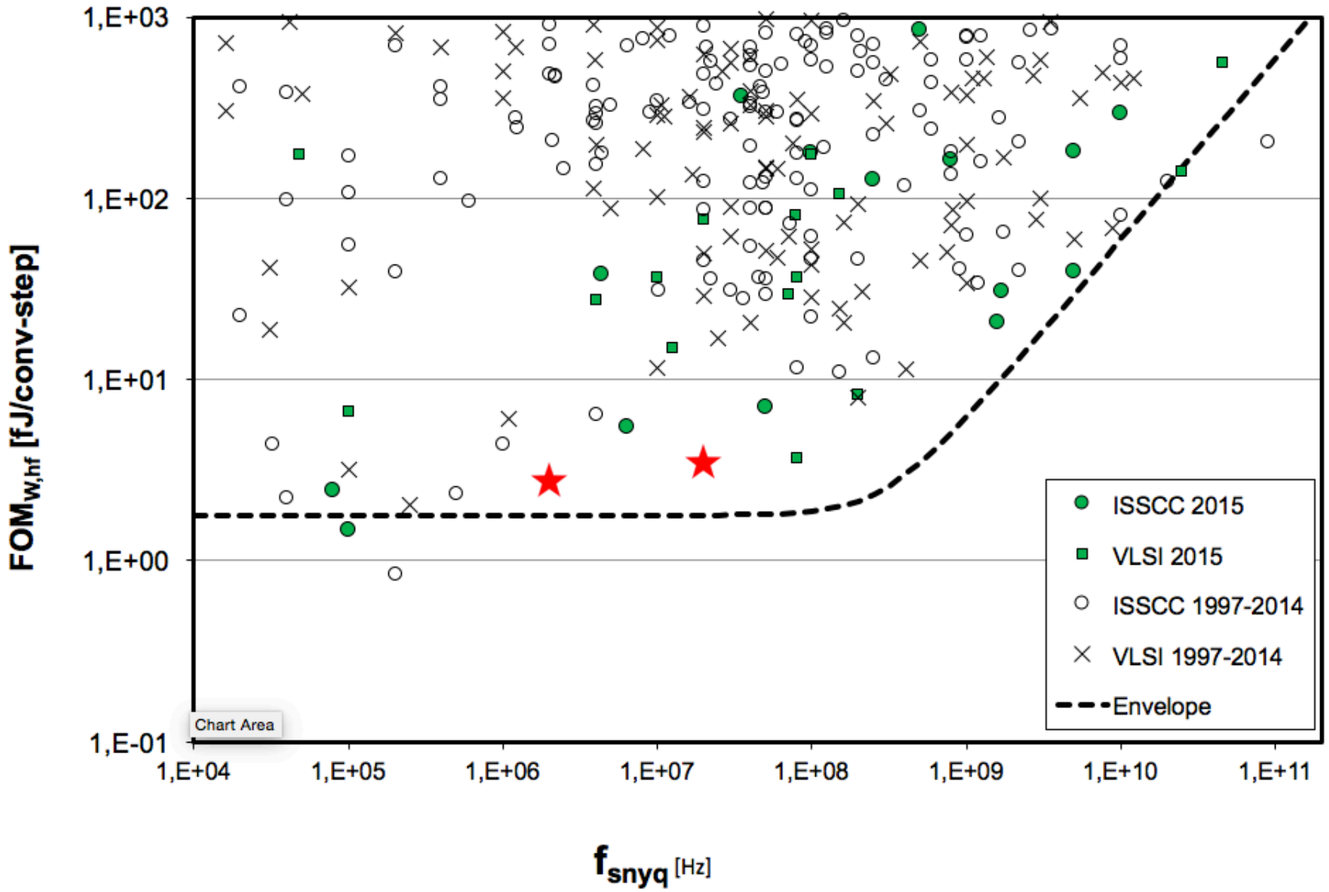


First tapeout (Jan 2015)[1]



[1] To read more on the two 9-bit ADCs, see proceedings from ESSCIRC 2016

Comparison to state-of-the art




Game menu
Back to Game
Achievements
Statistics
Options...
Open to LAN
Disconnect

Want to help me make better EDA tools?

And have fun at the same time.

http://www.github.com/wulffern/ciccreator

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