# Making integrated circuits

2014-03-20, Carsten Wulff

# Topic for today

- How do we make integrated circuits
- What to focus on the next five years

# Who am I

- Carsten Wulff
- Senior R & D engineer at Nordic Semiconductor (3 days a week)
- Post. doc at NTNU (2 days a week)
- Married with three kids
- Master (2002), Ph.D (2008)

# What do I do at Nordic?

Analog integrated circuit design, mostly analog to digital converters

NORDIC SEMICONDUCTOR

## nRF51822

Multiprotocol *Bluetooth*® 4.0 low energy/2.4 GHz RF SoC

## Product Specification v1.1

### Key Features

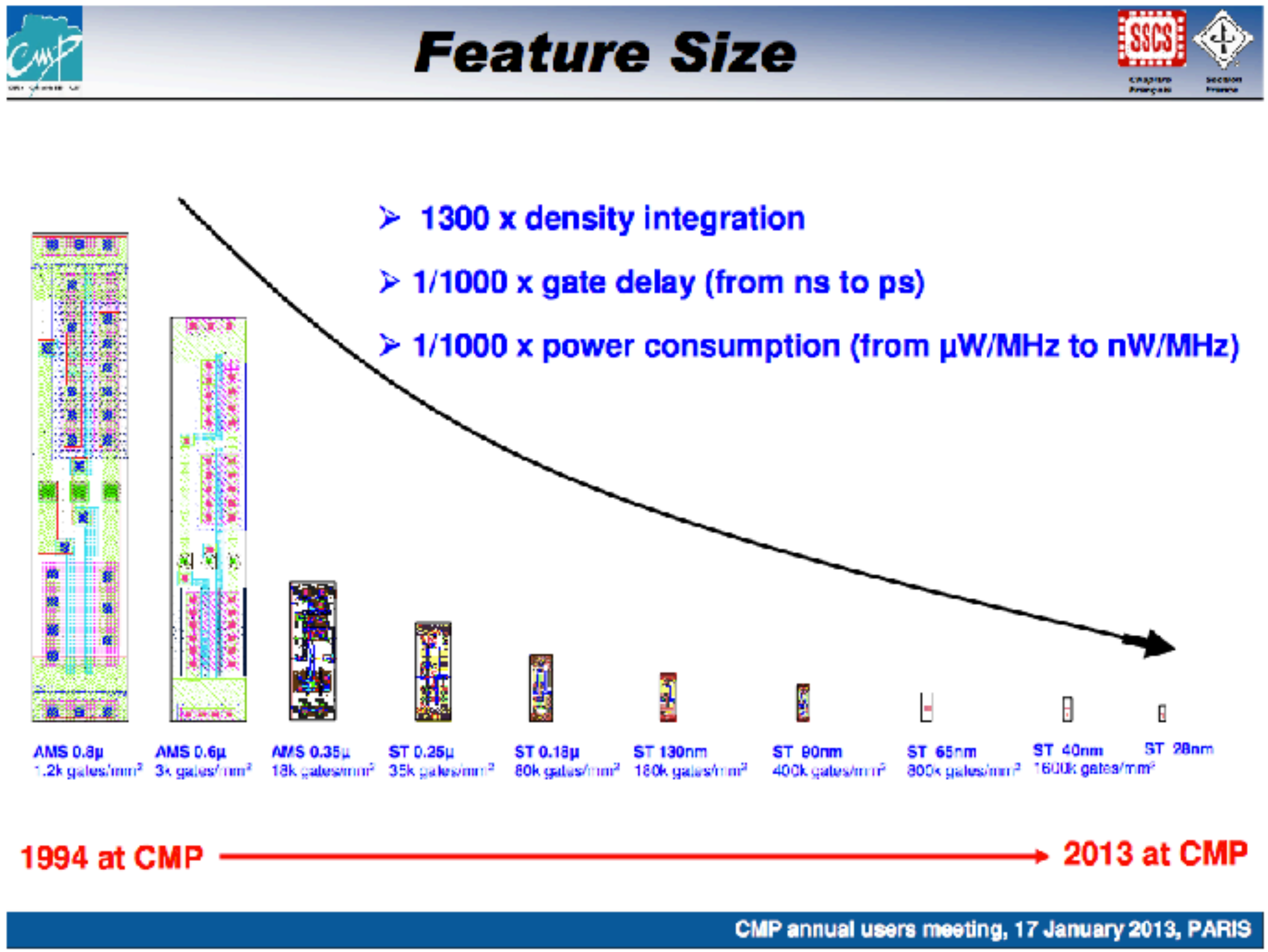
- 2.4 GHz transceiver
  - -93 dBm sensitivity *Bluetooth*® low energy
  - 250 kbps, 1 Mbps, 2 Mbps supported data rates
  - TX Power -20 to +4 dBm in 4 dB steps
  - TX Power -30 dBm Whisper mode
  - 13 mA peak RX, 10.5 mA peak TX (0 dBm)
  - RSSI (1 dB resolution)
- ARM® Cortex™-M0 32 bit processor
  - 275 µA/MHz running from flash memory
  - 150 µA/MHz running from RAM
  - Serial Wire Debug (SWD)
- S100 series SoftDevice ready
- Memory
  - 256 kB or 128 kB embedded flash program memory
  - 16 kB RAM
- Support for non-concurrent multiprotocol operation
  - On-air compatibility with nRF24L series
- Flexible Power Management
  - Supply voltage range 1.8 V to 3.6 V
  - 2.5 µs fast wake-up using 16 MHz RCOSC
  - 0.4 µA @ 3 V OFF mode
  - 0.5 µA @ 3 V in OFF mode + 1 region RAM retention
  - 2.3 µA @ 3 V ON mode, all blocks IDLE
- 8/9/10 bit ADC - 8 configurable channels
- 31 General Purpose I/O Pins
- Two 16 bit and one 32 bit timers with counter mode
- SPI Master

### Applications

- Computer peripherals anc
  - Mouse
  - Keyboard
  - Multi-touch
- Interactive entertainment
  - Remote cor
  - 3D Glasses
  - Gaming cor
- Personal Area Networks
  - Health and monitor de
  - Medical dev
  - Key-fobs +
- Remote control toys

# What do I do at NTNU?

Analog to digital converters in advanced CMOS technologies.




http://cmp.imag.fr/aboutus/slides/Slides2013/05_ST_2013.pdf

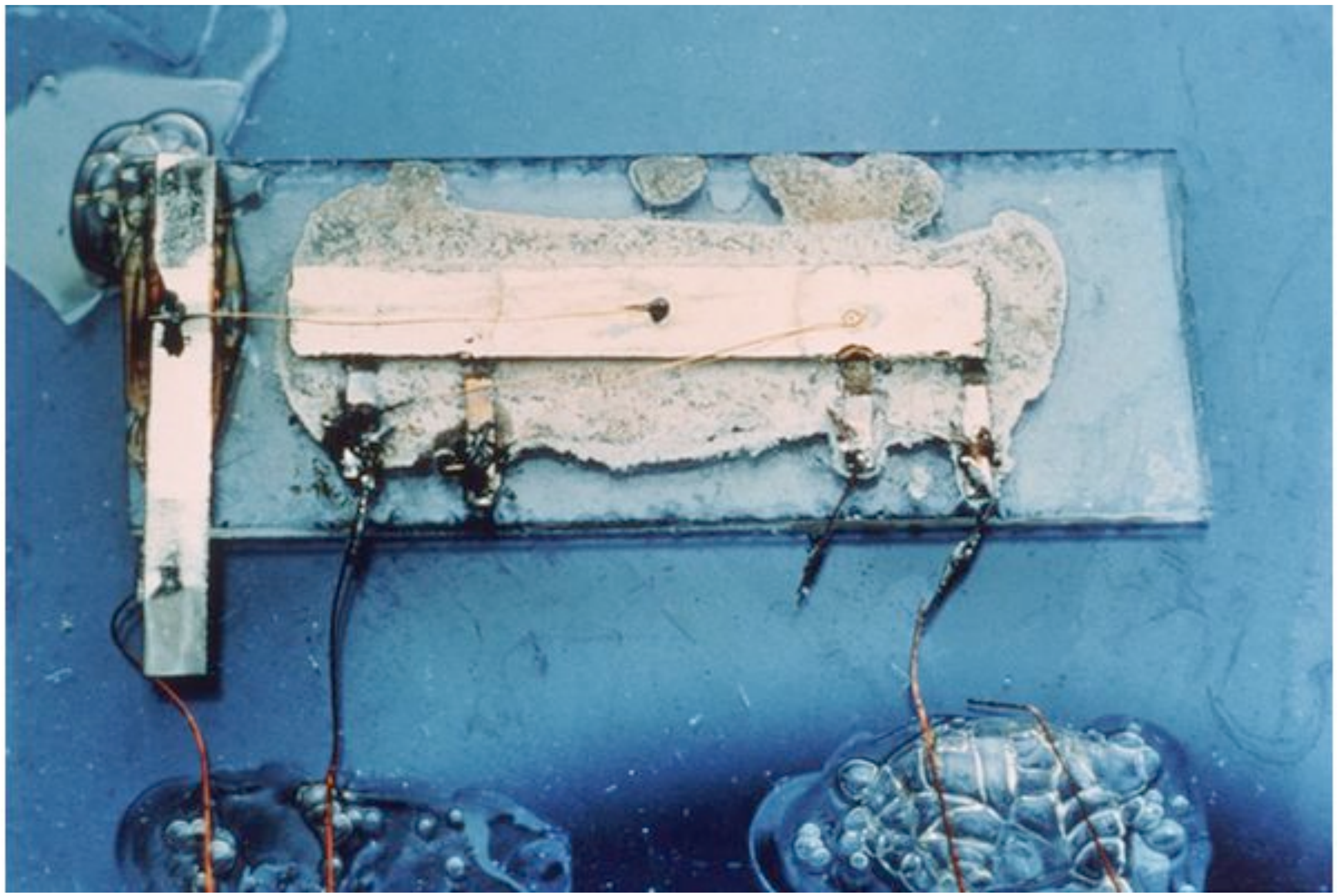
# How do we make integrated circuits?

# Transistor

# 1947: First transistor

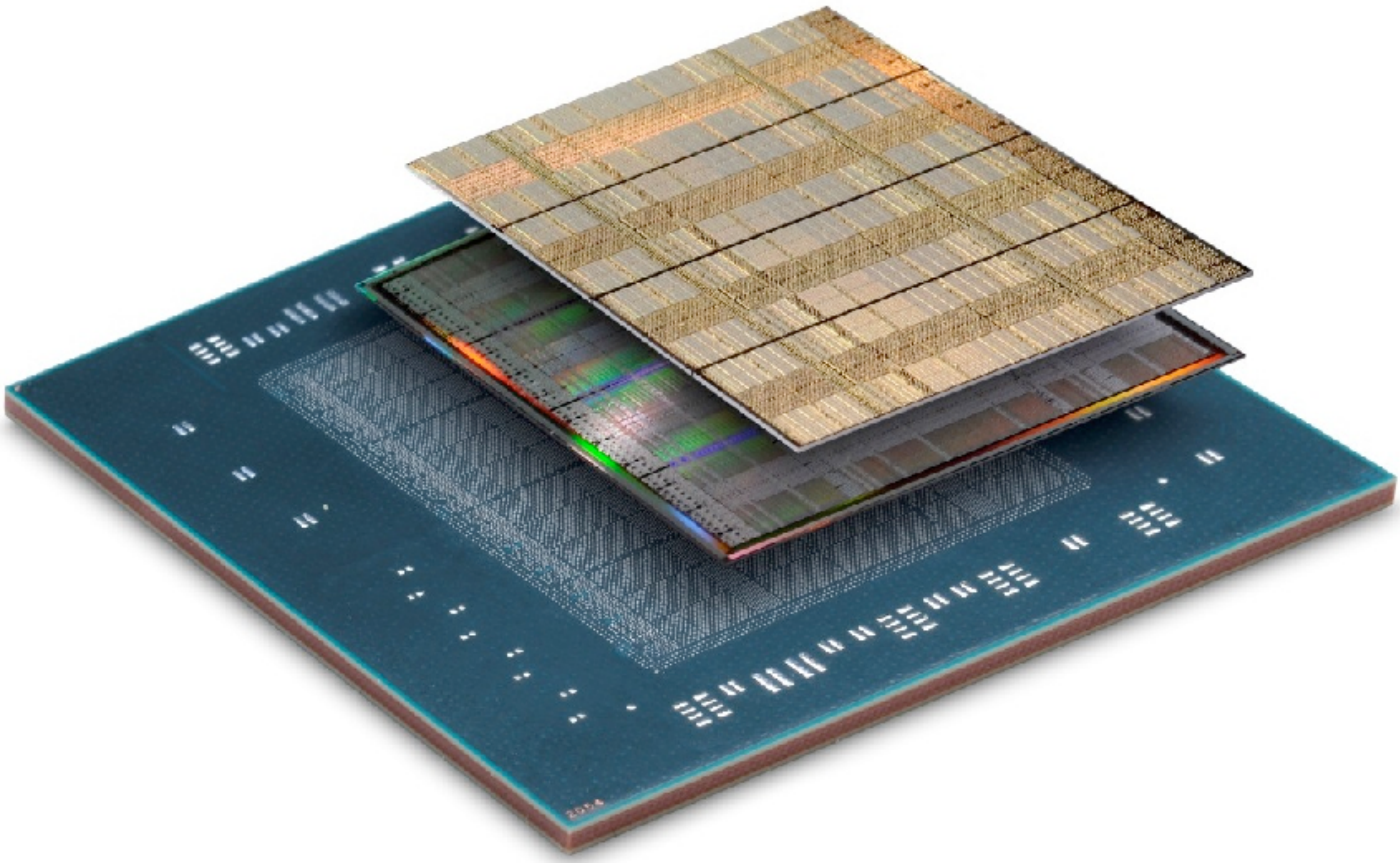
http://www.beatriceco.com/bti/porticus/bell/belllabs_transistor.html

# 1958: Integrated circuit



http://en.wikipedia.org/wiki/Jack_Kilby

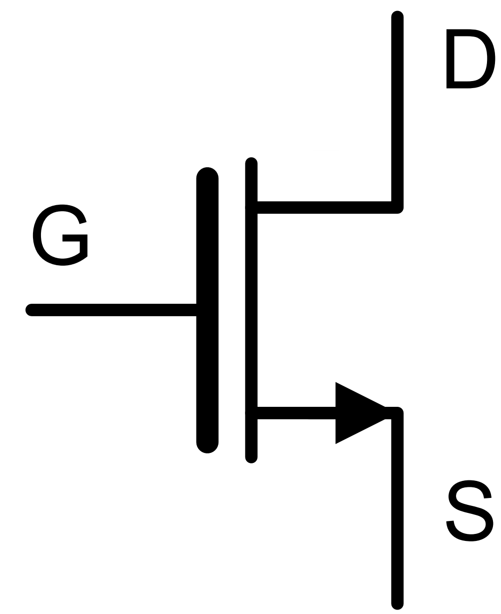
# Xilinx Virtex-7



**6.8 Billion transistors**

# Transistor

- The most important device in an integrated circuit.
- An extremely complicated device
- Need computer models to describe the behavior accurately.
- BSIM model published in 1987, 17 parameters to describe a transistor. This is similar what you find in textbooks. Applies to 1um transistor lengths.






IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. SC-22, NO. 4, AUGUST 1987

## BSIM: Berkeley Short-Channel IGFET Model for MOS Transistors

BING J. SHEU, MEMBER, IEEE, DONALD L. SCHARFETTER, FELLOW, IEEE, PING-KEUNG KO, MEMBER, IEEE, AND MIN-CHIE JENG

*Abstract* —The Berkeley Short-channel IGFET Model (BSIM), an accurate and computationally efficient MOS transistor model, and its associated characterization facility for advanced integrated-circuit design are described. Both the strong-inversion and weak-inversion components of the drain-current expression are included. In order to speed up the circuit-simulation execution time, the dependence of the drain current on the substrate bias has been modeled with a numerical approximation. This approximation also simplifies the transistor terminal charge expressions. The charge model was derived from its drain-current counterpart to

only as accurate as the models used. In the past, the SPICE2 program has provided three built-in MOS transistor models [6]. The Level-1 model, which contains fairly simple expressions, is most suitable for preliminary analysis. The Level-2 model, which contains expressions from detailed device physics, does not work well for small-geometry transistors. The Level-3 model represents an attempt to pursue the semi-empirical modeling approach

*3. Saturation Region* $[V_{GS} > V_{th}$ *and* $V_{DS} \geqslant V_{D\,\mathrm{SAT}}]$:

$$I_{DS} = \frac{\mu_0}{[1 + U_0(V_{GS} - V_{th})]} \cdot \frac{C_{ox}\frac{W}{L}(V_{GS} - V_{th})^2}{2aK}$$

# BSIM 4.5 = 284 parameters

.MODEL N1 NMOS LEVEL=14 VERSION=4.5.0 BINUNIT=1 PARAMCHK=1 MOBMOD=0 CAPMOD=2 IGCMOD=1 IGBMOD=1 GEOMOD=1 DIOMOD=1 RDSMOD=0 RBODYMOD=0 RGATEMOD=3 PERMOD=1 ACNQSMOD=0 TRNQSMOD=0 TEMPMOD=0 TNOM=27 **TOXE=1.8E-009** TOXP=10E-010 TOXM=1.8E-009 DTOX=8E-10 EPSROX=3.9 WINT=5E-009 LINT=1E-009 LL=0 WL=0 LLN=1 WLN=1 LW=0 WW=0 LWN=1 WWN=1 LWL=0 WWL=0 XPART=0 TOXREF=1.4E-009 SAREF=5E-6 SBREF=5E-6 WLOD=2E-6 KU0=-4E-6 KVSAT=0.2 KVTH0=-2E-8 TKU0=0.0 LLODKU0=1.1 WLODKU0=1.1 LLODVTH=1.0 WLODVTH=1.0 LKU0=1E-6 WKU0=1E-6 PKU0=0.0 LKVTH0=1.1E-6 WKVTH0=1.1E-6 PKVTH0=0.0 STK2=0.0 LODK2=1.0 STETA0=0.0 LODETA0=1.0 LAMBDA=4E-10 VSAT=1.1E 005 VTL=2.0E5 XN=6.0 LC=5E-9 RNOIA=0.577 RNOIB=0.37 LINTNOI=1E-009 WPEMOD=0 WEB=0.0 WEC=0.0 KVTH0WE=1.0 K2WE=1.0 KU0WE=1.0 SCREF=5.0E-6 TVOFF=0.0 TVFBSDOFF=0.0 **VTH0=0.25** K1=0.35 K2=0.05 K3=0 K3B=0 W0=2.5E-006 DVT0=1.8 DVT1=0.52 DVT2=-0.032 DVT0W=0 DVT1W=0 DVT2W=0 DSUB=2 MINV=0.05 VOFFL=0 DVTP0=1E-007 DVTP1=0.05 LPE0=5.75E-008 LPEB=2.3E-010 XJ=2E-008 NGATE=5E 020 NDEP=2.8E 018 NSD=1E 020 PHIN=0 CDSC=0.0002 CDSCB=0 CDSCD=0 CIT=0 VOFF=-0.15 NFACTOR=1.2 ETA0=0.05 ETAB=0 UC=-3E-011 VFB=-0.55 **U0=0.032** UA=5.0E-011 UB=3.5E-018 A0=2 AGS=1E-020 A1=0 A2=1 B0=-1E-020 B1=0 KETA=0.04 DWG=0 DWB=0 PCLM=0.08 PDIBLC1=0.028 PDIBLC2=0.022 PDIBLCB=-0.005 DROUT=0.45 PVAG=1E-020 DELTA=0.01 PSCBE1=8.14E 008 PSCBE2=5E-008 RSH=0 RDSW=0 RSW=0 RDW=0 FPROUT=0.2 PDITS=0.2 PDITSD=0.23 PDITSL=2.3E 006 RSH=0 RDSW=50 RSW=150 RDW=150 RDSWMIN=0 RDWMIN=0 RSWMIN=0 PRWG=0 PRWB=6.8E-011 WR=1 ALPHA0=0.074 ALPHA1=0.005 BETA0=30 AGIDL=0.0002 BGIDL=2.1E 009 CGIDL=0.0002 EGIDL=0.8 AIGBACC=0.012 BIGBACC=0.0028 CIGBACC=0.002 NIGBACC=1 AIGBINV=0.014 BIGBINV=0.004 CIGBINV=0.004 EIGBINV=1.1 NIGBINV=3 AIGC=0.012 BIGC=0.0028 CIGC=0.002 AIGSD=0.012 BIGSD=0.0028 CIGSD=0.002 NIGC=1 POXEDGE=1 PIGCD=1 NTOX=1 VFBSDOFF=0.0 XRCRG1=12 XRCRG2=5 CGSO=6.238E-010 CGDO=6.238E-010 CGBO=2.56E-011 CGDL=2.495E-10 CGSL=2.495E-10 CKAPPAS=0.03 CKAPPAD=0.03 ACDE=1 MOIN=15 NOFF=0.9 VOFFCV=0.02 KT1=-0.37 KT1L=0.0 KT2=-0.042 UTE=-1.5 UA1=1E-009 UB1=-3.5E-019 UC1=0 PRT=0 AT=53000 FNOIMOD=1 TNOIMOD=0 JSS=0.0001 JSWS=1E-011 JSWGS=1E-010 NJS=1 IJTHSFWD=0.01 IJTHSREV=0.001 BVS=10 XJBVS=1 JSD=0.0001 JSWD=1E-011 JSWGD=1E-010 NJD=1 IJTHDFWD=0.01 IJTHDREV=0.001 BVD=10 XJBVD=1 PBS=1 CJS=0.0005 MJS=0.5 PBSWS=1 CJSWS=5E-010 MJSWS=0.33 PBSWGS=1 CJSWGS=3E-010 MJSWGS=0.33 PBD=1 CJD=0.0005 MJD=0.5 PBSWD=1 CJSWD=5E-010 MJSWD=0.33 PBSWGD=1 CJSWGD=5E-010 MJSWGD=0.33 TPB=0.005 TCJ=0.001 TPBSW=0.005 TCJSW=0.001 TPBSWG=0.005 TCJSWG=0.001 XTIS=3 XTID=3 DMCG=0E-006 DMCI=0E-006 DMDG=0E-006 DMCGT=0E-007 DWJ=0.0E-008 XGW=0E-007 XGL=0E-008 RSHG=0.4 GBMIN=1E-010 RBPB=5 RBPD=15 RBPS=15 RBDB=15 RBSB=15 NGCON=1 JTSS=1E-4 JTSD=1E-4 JTSSWS=1E-10 JTSSWD=1E-10 JTSSWGS=1E-7 JTSSWGD=1E-7 NJTS=20.0 NJTSSW=20 NJTSSWG=6 VTSS=10 VTSD=10 VTSSWS=10 VTSSWD=10 VTSSWGS=2 VTSSWGD=2 XTSS=0.02 XTSD=0.02 XTSSWS=0.02 XTSSWD=0.02 XTSSWGS=0.02 XTSSWGD=0.02

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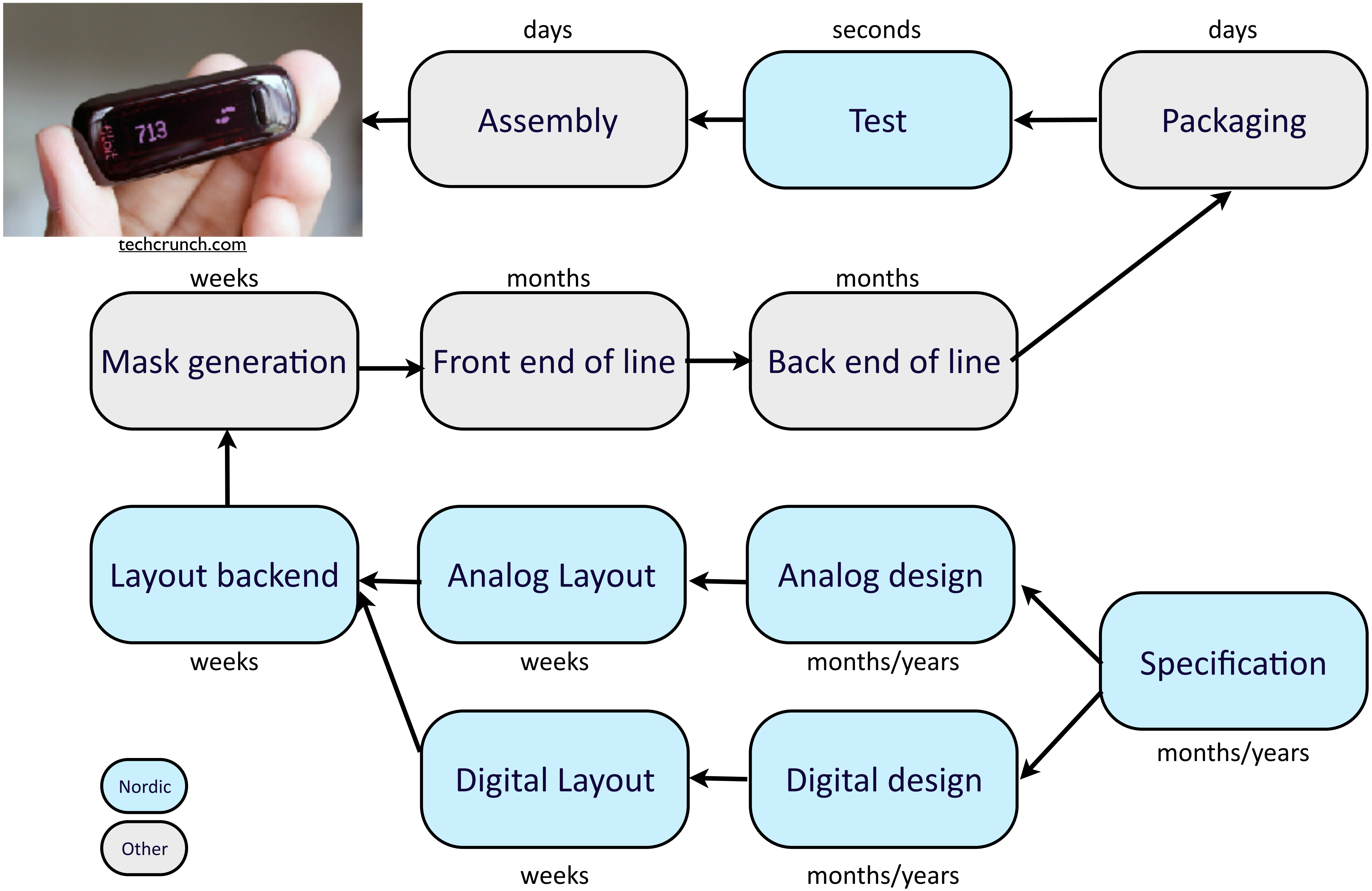
# Lesson 1

It's not practical to do accurate hand calculation for transistors.  Finding where to start will have to do

# The story

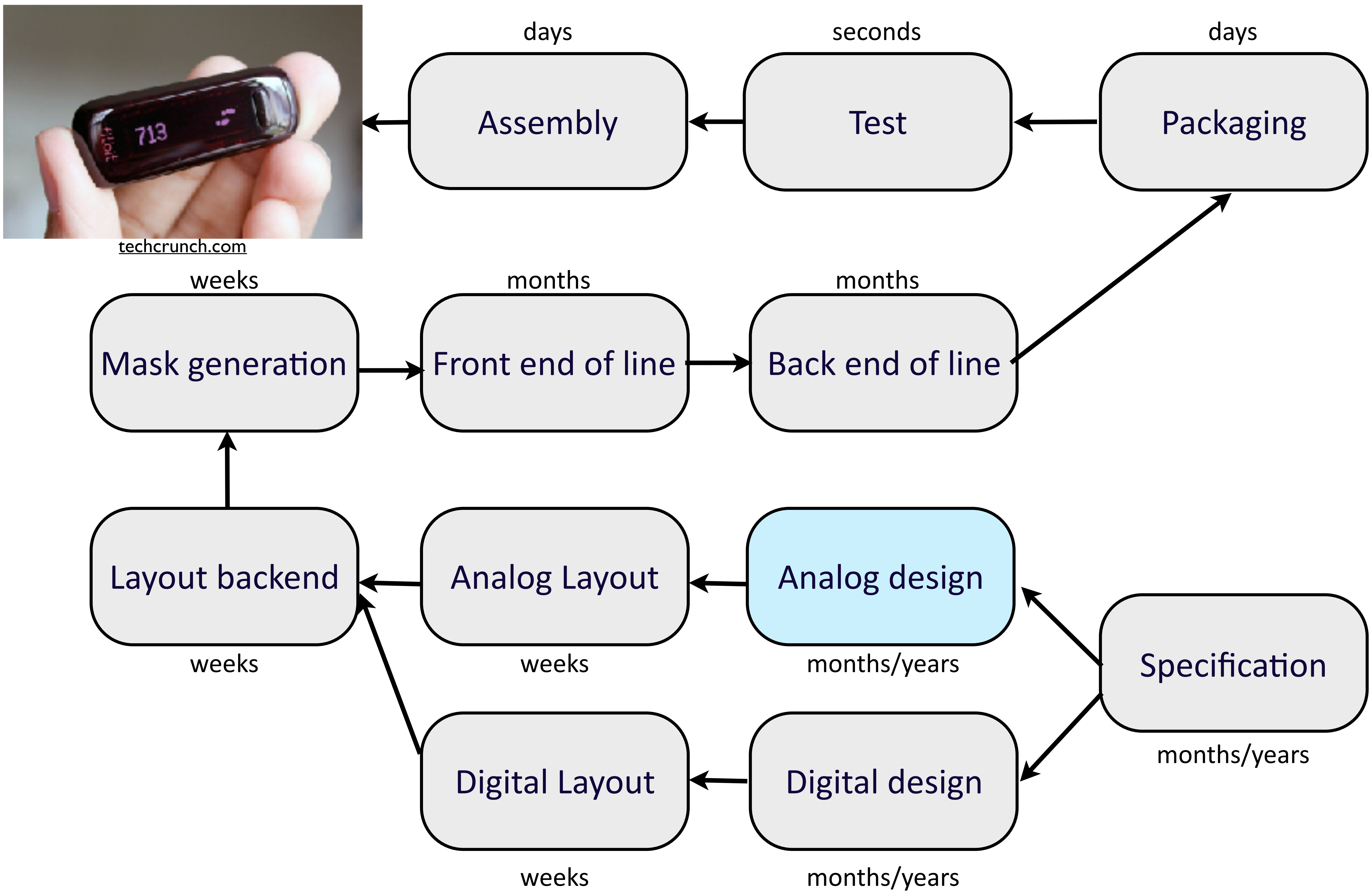
# The complete story



# Specification

- Trying to figure out what we need to make
- Maybe the most difficult step in the process, because were trying to guess what customers need 2-3 years before they need it.
- Usually done by the senior designers

# The complete story



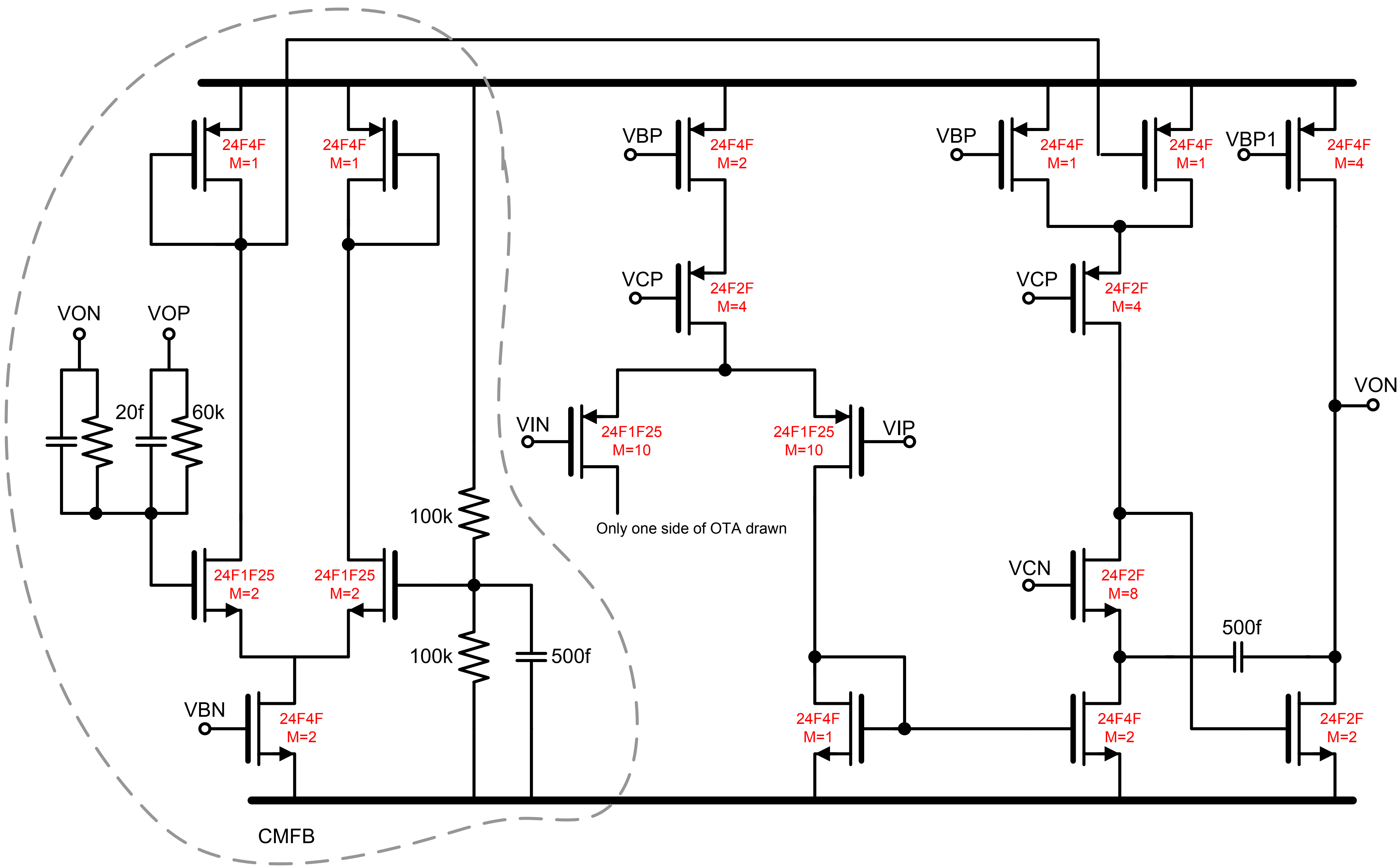
## Demo: Design of an analog-to-digital converter

- 8-bit converter
- Does not need to be fast (kHz)
- Current is not that important (300uA)
- It must be small
- Must use 16MHz clock

# Transistor design tips

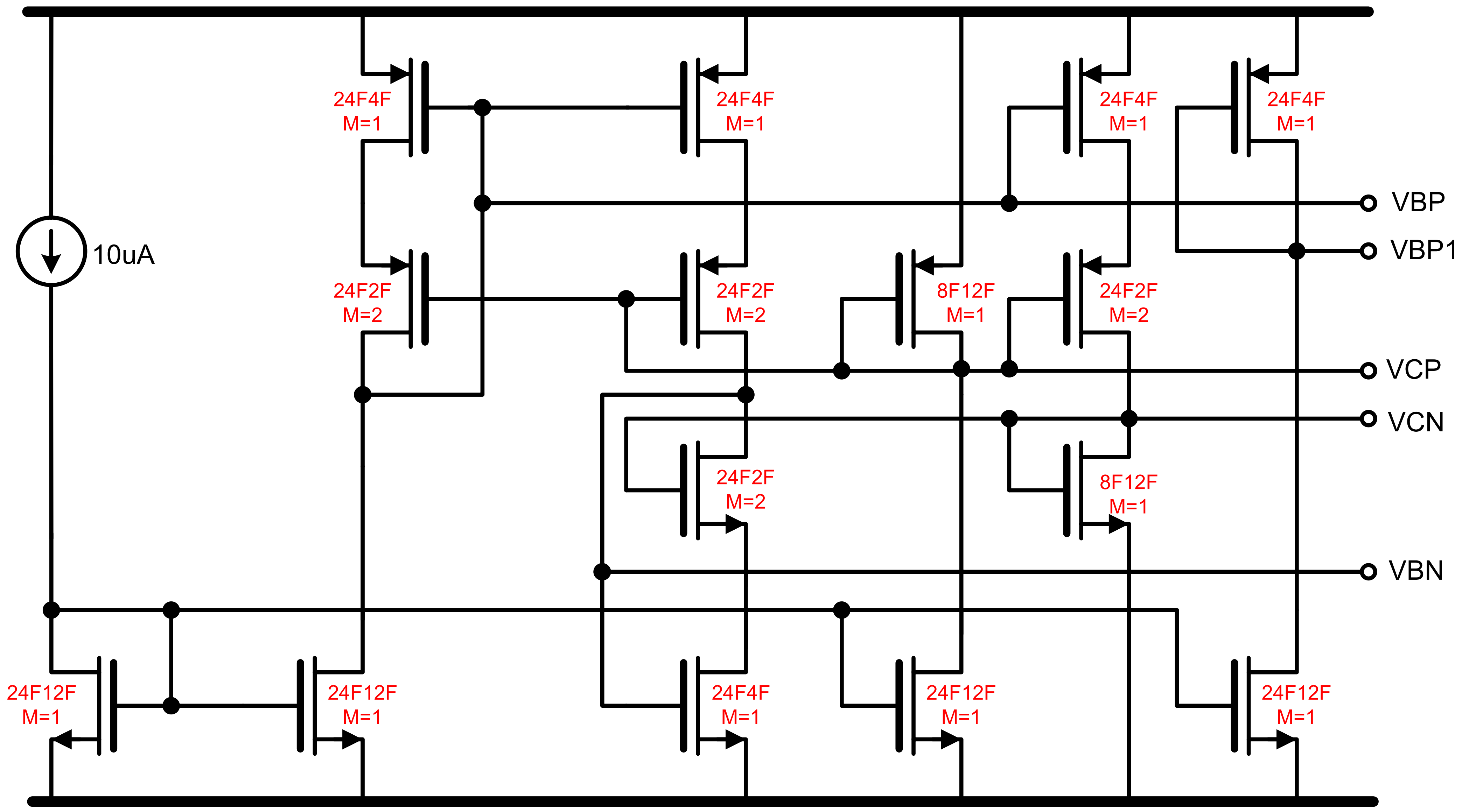
- NMOS ~ 2uA - 10 uA per square. For example W=20F L=2F ~ 100uA (F = minimum gate length)
- PMOS ~ 0.5uA - 3uA per square
- Width ~ 1 - 20 times the lengths

# Differential OTA with CT CMFB

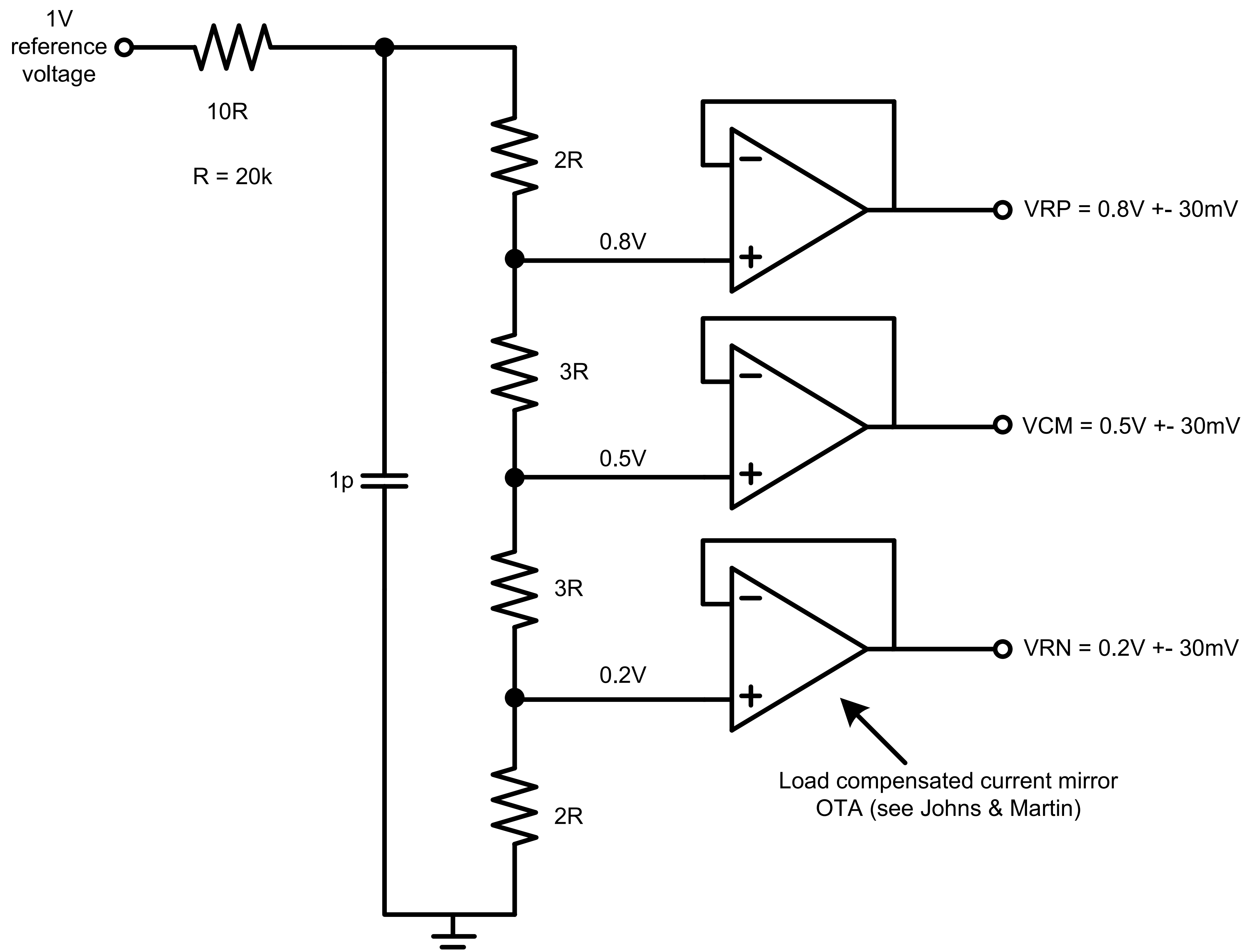



F = minimum transistor gate length. For example 24F4F => W = 24 x min gate, L= 4 x min gate

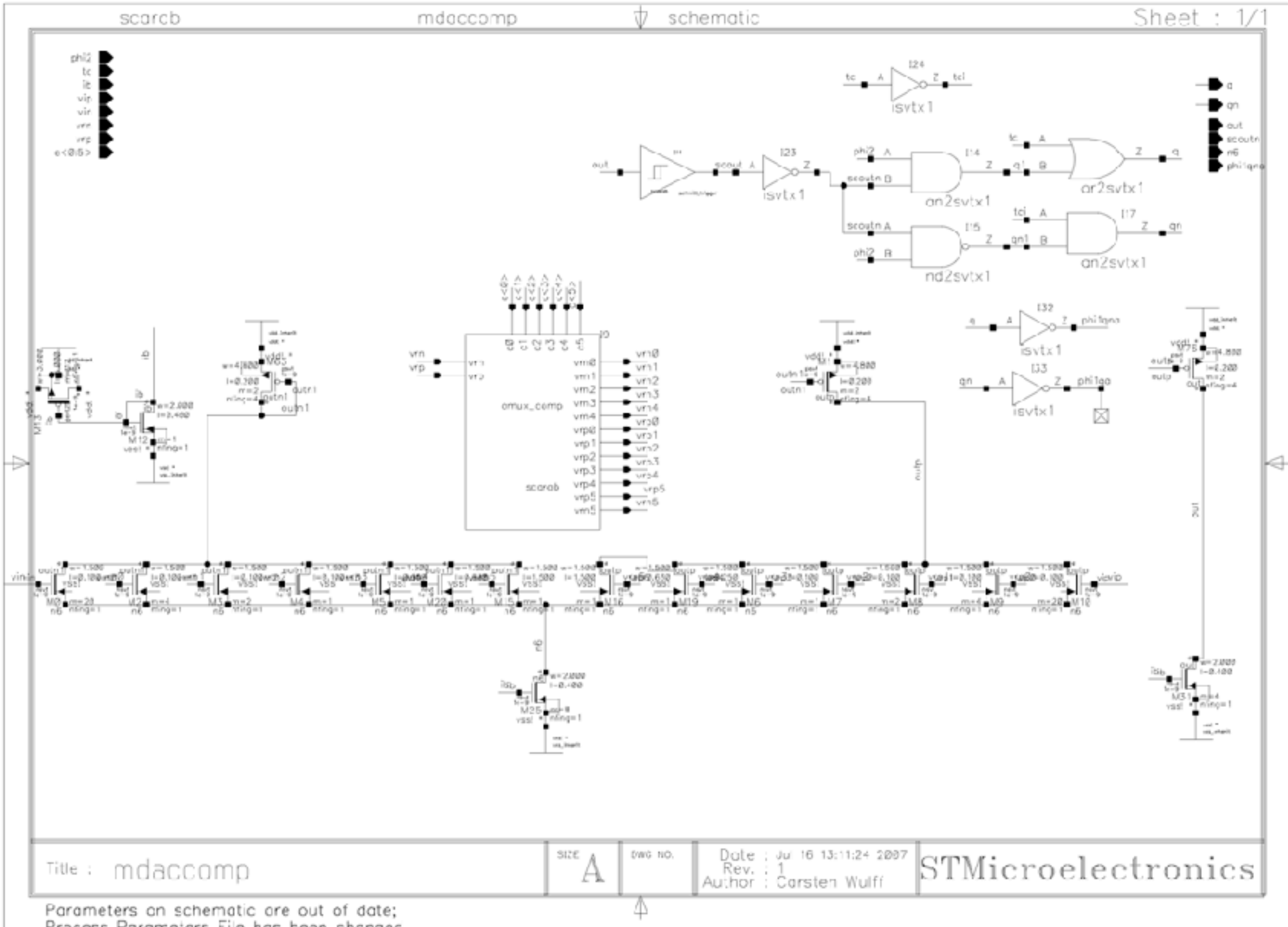
# Differential OTA - Bias circuit



# Voltage divider



# Schematic

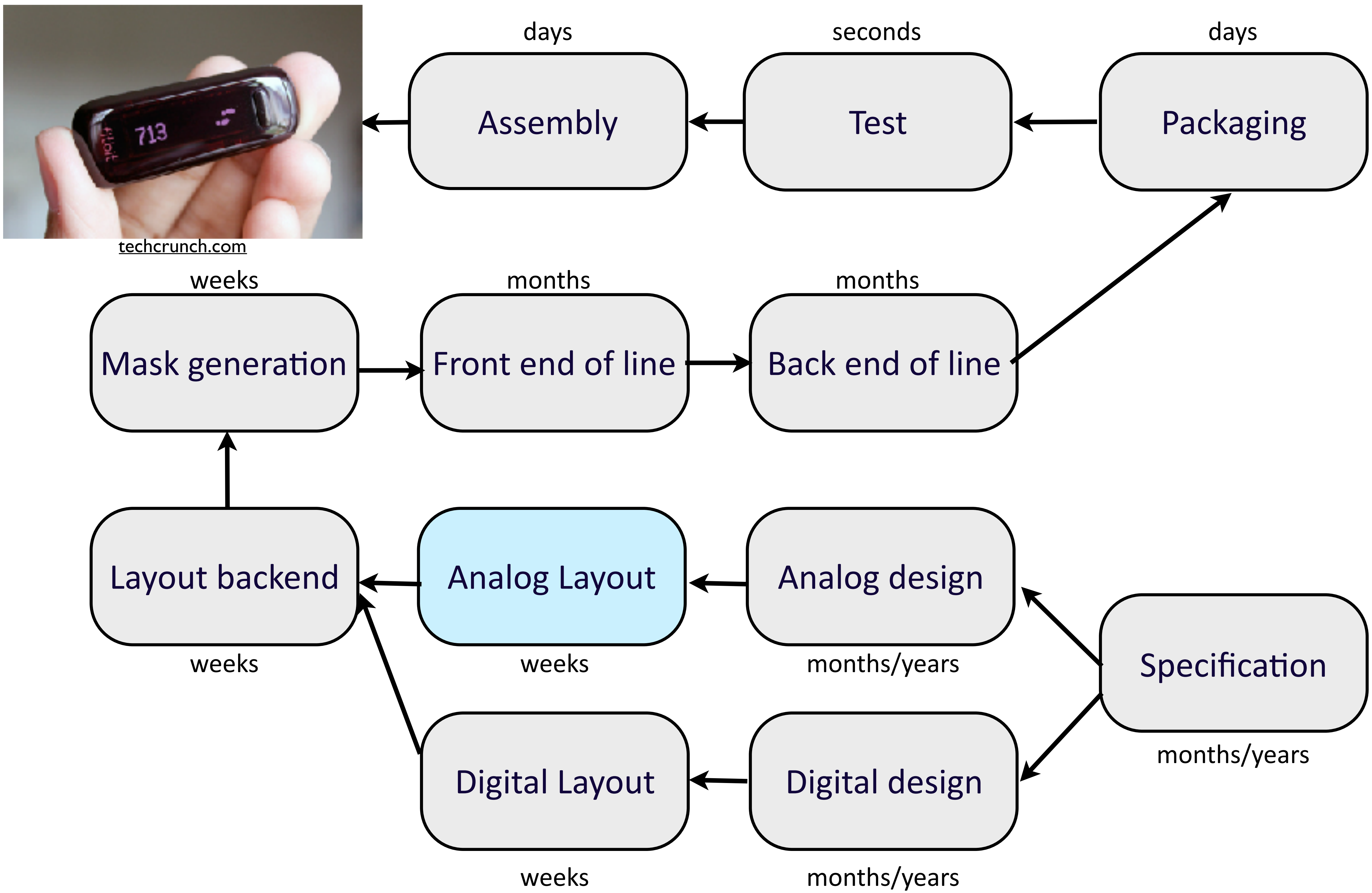



You can download the complete ADC from www.wulff.no/carsten

# Netlist

```
.subckt SeCmOTA IN  IP  IB  VDA  VDB  VS  VM  VO  AVDD  AVSS  M=1
  MNCHC10F12_0    IB  IB  AVSS  AVSS  nch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MNCHC10F12_1    IB  IB  AVSS  AVSS  nch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MNCHC10F12_2    IB  IB  AVSS  AVSS  nch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MNCHC10F12_3    IB  IB  AVSS  AVSS  nch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MNCHC10F12_4    VS  IB  AVSS  AVSS  nch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MNCHC10F12_5    VS  IB  AVSS  AVSS  nch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MNCHC10F12_6    VS  IB  AVSS  AVSS  nch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MNCHC10F12_7    VS  IB  AVSS  AVSS  nch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MPCHC10F12_8    VDA  VDA  AVDD  AVDD  pch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MPCHC10F12_9    VDA  VDA  AVDD  AVDD  pch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MPCHC10F12_10    VDA  VDA  AVDD  AVDD  pch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MPCHC10F12_11    VDA  VDA  AVDD  AVDD  pch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MPCHC10F12_12    VM  VDA  AVDD  AVDD  pch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MPCHC10F12_13    VDB  VDB  AVDD  AVDD  pch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MPCHC10F12_14    VDB  VDB  AVDD  AVDD  pch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MPCHC10F12_15    VDB  VDB  AVDD  AVDD  pch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MPCHC10F12_16    VDB  VDB  AVDD  AVDD  pch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MPCHC10F12_17    VO  VDB  AVDD  AVDD  pch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MNCHC10F12_18    VM  VM  AVSS  AVSS  nch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MNCHC10F12_19    VM  VM  AVSS  AVSS  nch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MNCHC10F12_20    VM  VM  AVSS  AVSS  nch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MNCHC10F12_21    VM  VM  AVSS  AVSS  nch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MNCHC10F12_22    VO  VM  AVSS  AVSS  nch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MNCHC10F12_23    VO  VM  AVSS  AVSS  nch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MNCHC10F12_24    VO  VM  AVSS  AVSS  nch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MNCHC10F12_25    VO  VM  AVSS  AVSS  nch w=6.75e-06 l=2.16e-06 as=3.4425e-12 ad=4.86e-12 pd=8.19e-06 ps=1.452e-05 sa=5.1e-07 sb=4.11e-06 m=2 nrs=0.0755555555555555 nrd=0.106666666666667
  MNCHC4F1_26    VDA  IP  VS  AVSS  nch w=2.61e-06 l=1.8e-07 as=1.3311e-12 ad=1.8792e-12 pd=4.05e-06 ps=6.24e-06 sa=5.1e-07 sb=2.13e-06 m=2 nrs=0.195402298850575 nrd=0.275862068965517
  MNCHC4F1_27    VDA  IP  VS  AVSS  nch w=2.61e-06 l=1.8e-07 as=1.3311e-12 ad=1.8792e-12 pd=4.05e-06 ps=6.24e-06 sa=5.1e-07 sb=2.13e-06 m=2 nrs=0.195402298850575 nrd=0.275862068965517
  MNCHC4F1_28    VDA  IP  VS  AVSS  nch w=2.61e-06 l=1.8e-07 as=1.3311e-12 ad=1.8792e-12 pd=4.05e-06 ps=6.24e-06 sa=5.1e-07 sb=2.13e-06 m=2 nrs=0.195402298850575 nrd=0.275862068965517
  MNCHC4F1_29    VDA  IP  VS  AVSS  nch w=2.61e-06 l=1.8e-07 as=1.3311e-12 ad=1.8792e-12 pd=4.05e-06 ps=6.24e-06 sa=5.1e-07 sb=2.13e-06 m=2 nrs=0.195402298850575 nrd=0.275862068965517
  MNCHC4F1_30    VDA  IP  VS  AVSS  nch w=2.61e-06 l=1.8e-07 as=1.3311e-12 ad=1.8792e-12 pd=4.05e-06 ps=6.24e-06 sa=5.1e-07 sb=2.13e-06 m=2 nrs=0.195402298850575 nrd=0.275862068965517
  MNCHC4F1_31    VDA  IP  VS  AVSS  nch w=2.61e-06 l=1.8e-07 as=1.3311e-12 ad=1.8792e-12 pd=4.05e-06 ps=6.24e-06 sa=5.1e-07 sb=2.13e-06 m=2 nrs=0.195402298850575 nrd=0.275862068965517
  MNCHC4F1_32    VDA  IP  VS  AVSS  nch w=2.61e-06 l=1.8e-07 as=1.3311e-12 ad=1.8792e-12 pd=4.05e-06 ps=6.24e-06 sa=5.1e-07 sb=2.13e-06 m=2 nrs=0.195402298850575 nrd=0.275862068965517
  MNCHC4F1_33    VDA  IP  VS  AVSS  nch w=2.61e-06 l=1.8e-07 as=1.3311e-12 ad=1.8792e-12 pd=4.05e-06 ps=6.24e-06 sa=5.1e-07 sb=2.13e-06 m=2 nrs=0.195402298850575 nrd=0.275862068965517
  MNCHC4F1_34    VDB  IN  VS  AVSS  nch w=2.61e-06 l=1.8e-07 as=1.3311e-12 ad=1.8792e-12 pd=4.05e-06 ps=6.24e-06 sa=5.1e-07 sb=2.13e-06 m=2 nrs=0.195402298850575 nrd=0.275862068965517
  MNCHC4F1_35    VDB  IN  VS  AVSS  nch w=2.61e-06 l=1.8e-07 as=1.3311e-12 ad=1.8792e-12 pd=4.05e-06 ps=6.24e-06 sa=5.1e-07 sb=2.13e-06 m=2 nrs=0.195402298850575 nrd=0.275862068965517
  MNCHC4F1_36    VDB  IN  VS  AVSS  nch w=2.61e-06 l=1.8e-07 as=1.3311e-12 ad=1.8792e-12 pd=4.05e-06 ps=6.24e-06 sa=5.1e-07 sb=2.13e-06 m=2 nrs=0.195402298850575 nrd=0.275862068965517
  MNCHC4F1_37    VDB  IN  VS  AVSS  nch w=2.61e-06 l=1.8e-07 as=1.3311e-12 ad=1.8792e-12 pd=4.05e-06 ps=6.24e-06 sa=5.1e-07 sb=2.13e-06 m=2 nrs=0.195402298850575 nrd=0.275862068965517
  MNCHC4F1_38    VDB  IN  VS  AVSS  nch w=2.61e-06 l=1.8e-07 as=1.3311e-12 ad=1.8792e-12 pd=4.05e-06 ps=6.24e-06 sa=5.1e-07 sb=2.13e-06 m=2 nrs=0.195402298850575 nrd=0.275862068965517
  MNCHC4F1_39    VDB  IN  VS  AVSS  nch w=2.61e-06 l=1.8e-07 as=1.3311e-12 ad=1.8792e-12 pd=4.05e-06 ps=6.24e-06 sa=5.1e-07 sb=2.13e-06 m=2 nrs=0.195402298850575 nrd=0.275862068965517
  MNCHC4F1_40    VDB  IN  VS  AVSS  nch w=2.61e-06 l=1.8e-07 as=1.3311e-12 ad=1.8792e-12 pd=4.05e-06 ps=6.24e-06 sa=5.1e-07 sb=2.13e-06 m=2 nrs=0.195402298850575 nrd=0.275862068965517
  MNCHC4F1_41    VDB  IN  VS  AVSS  nch w=2.61e-06 l=1.8e-07 as=1.3311e-12 ad=1.8792e-12 pd=4.05e-06 ps=6.24e-06 sa=5.1e-07 sb=2.13e-06 m=2 nrs=0.195402298850575 nrd=0.275862068965517
.ends SeCmOTA
```

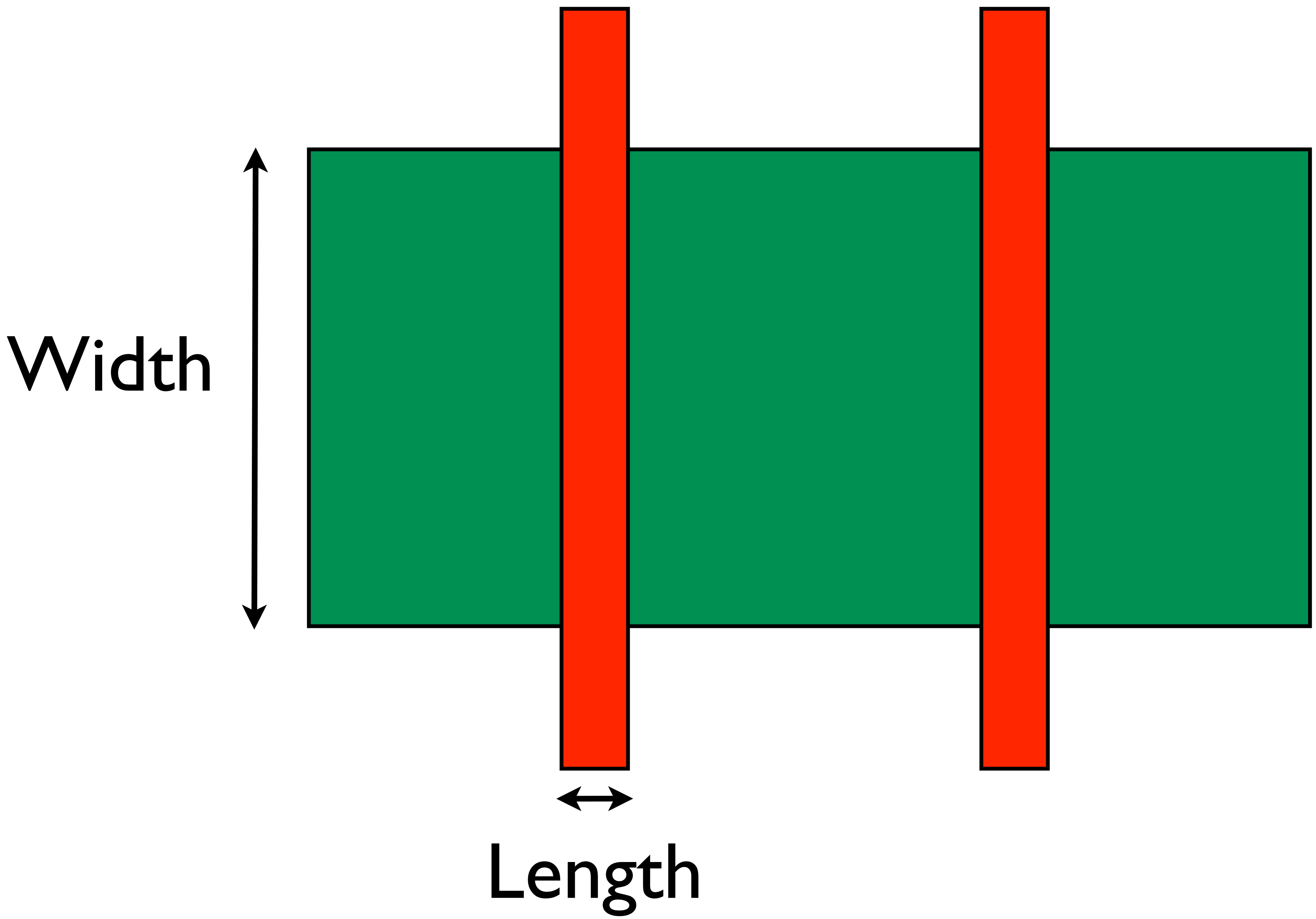
# The complete story



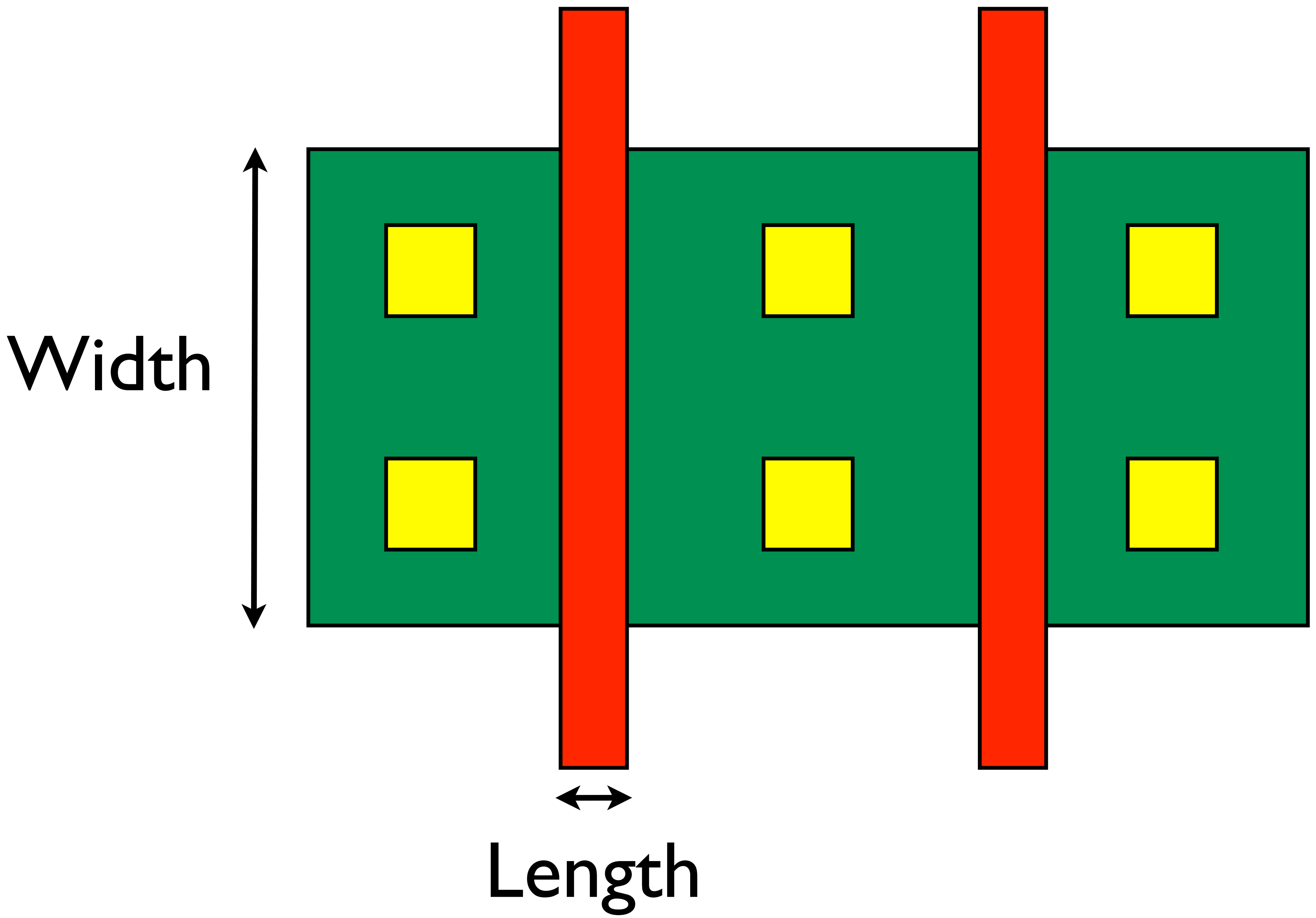
# Transistor layout - Diffusion


Marks the boundary of a transistor

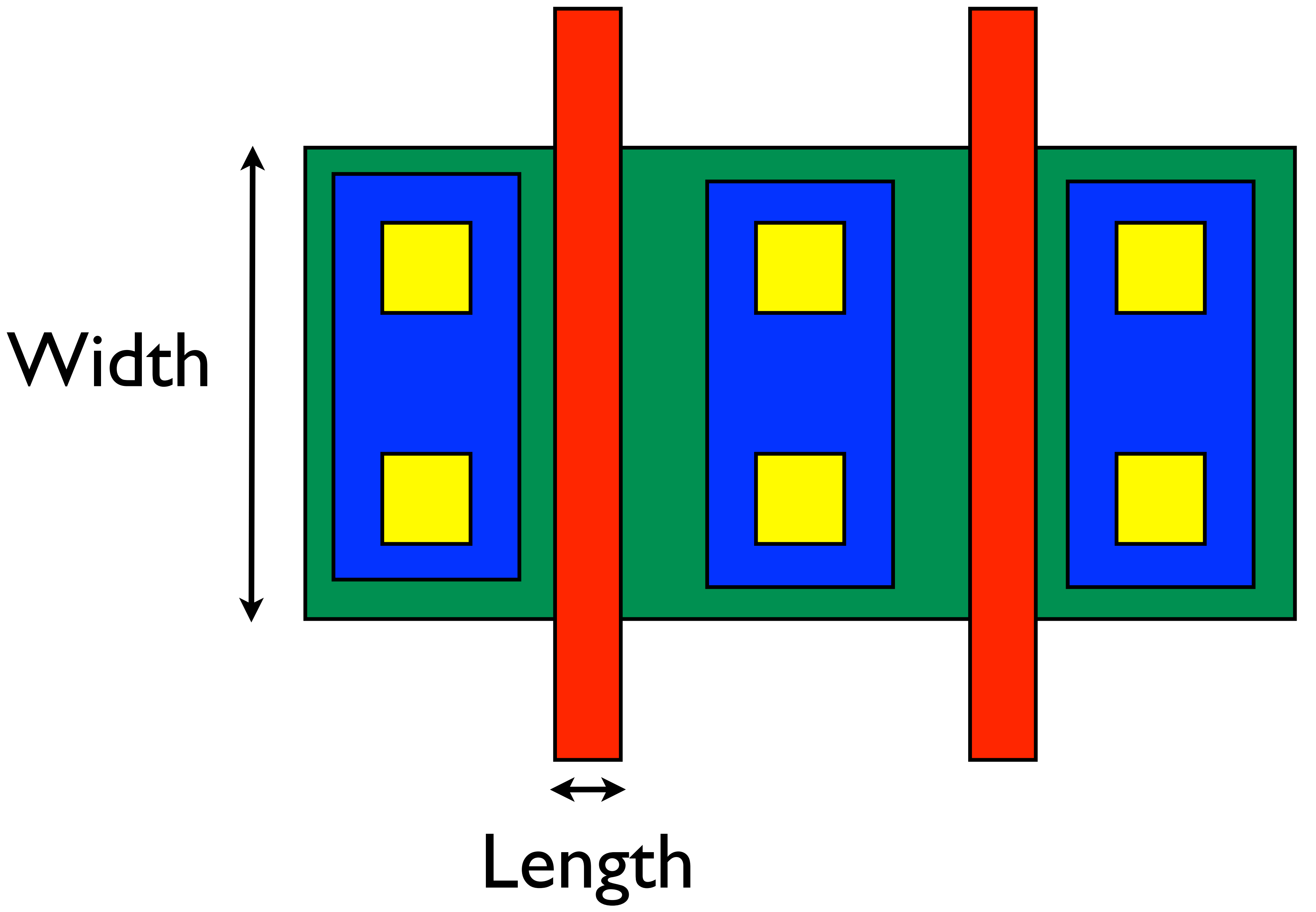
# Transistor layout - Gate

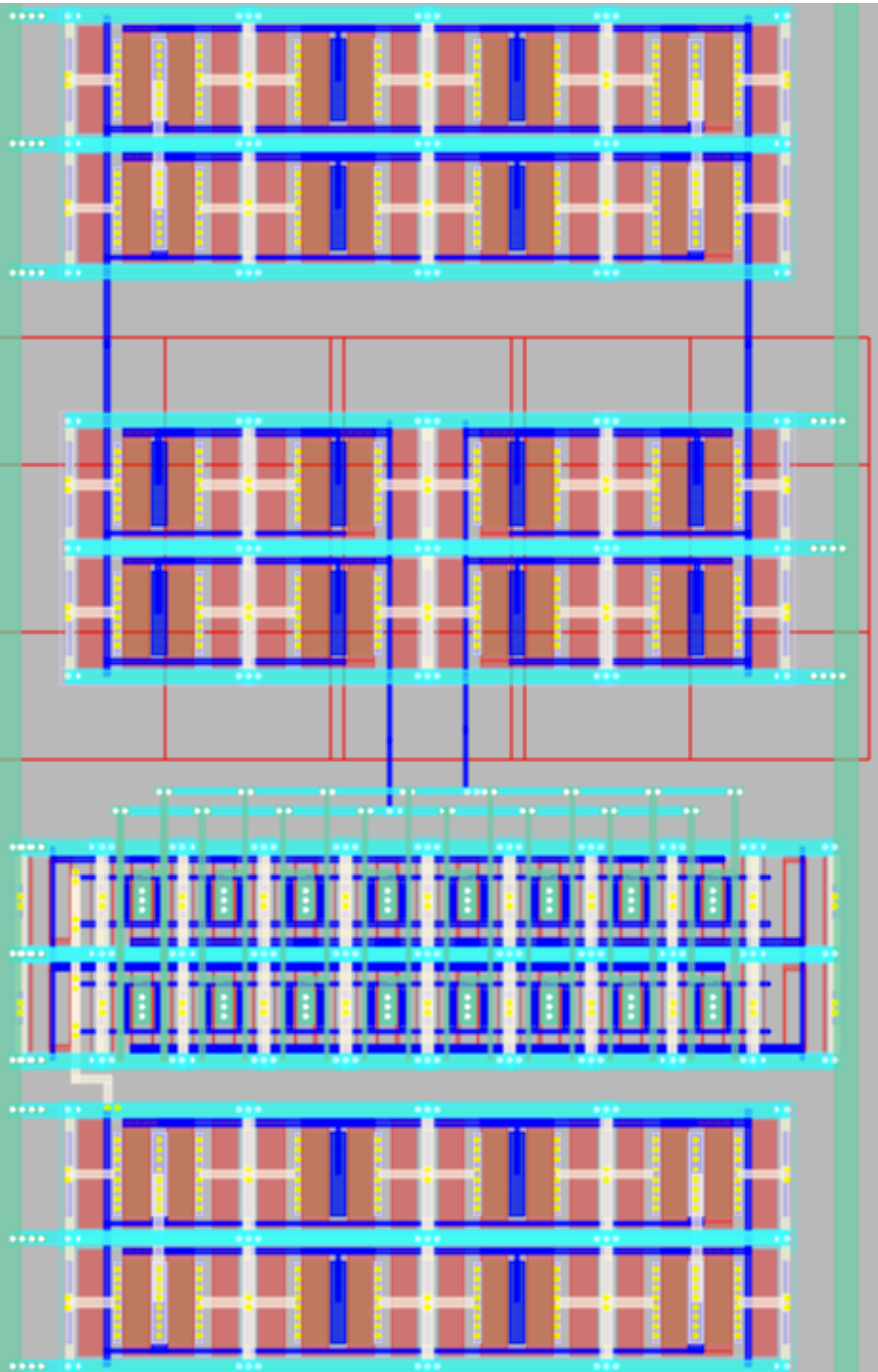


# Transistor layout - Contacts



# Transistor layout - Metal 1

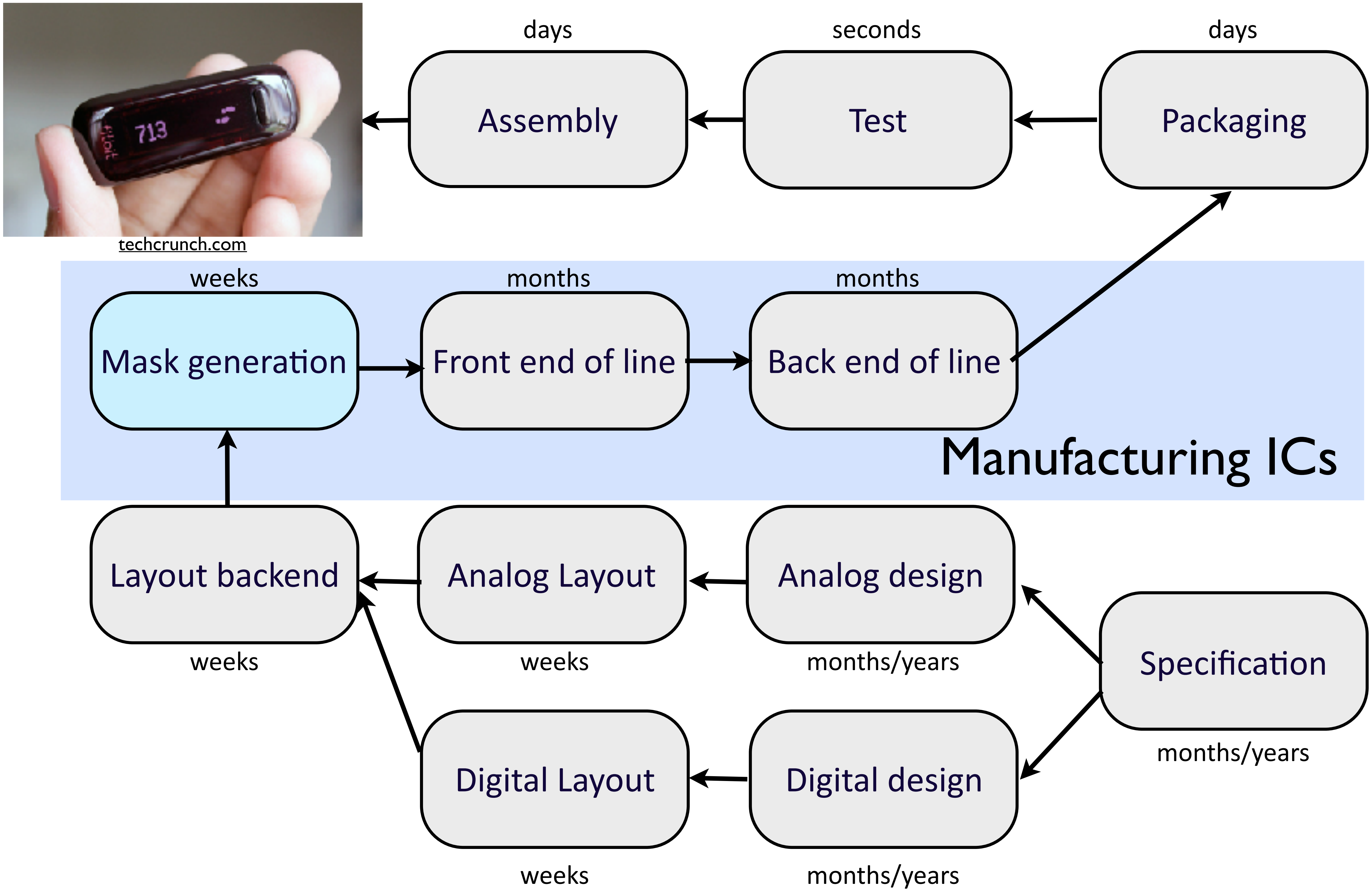




## Current mirror operational transconductance amplifier

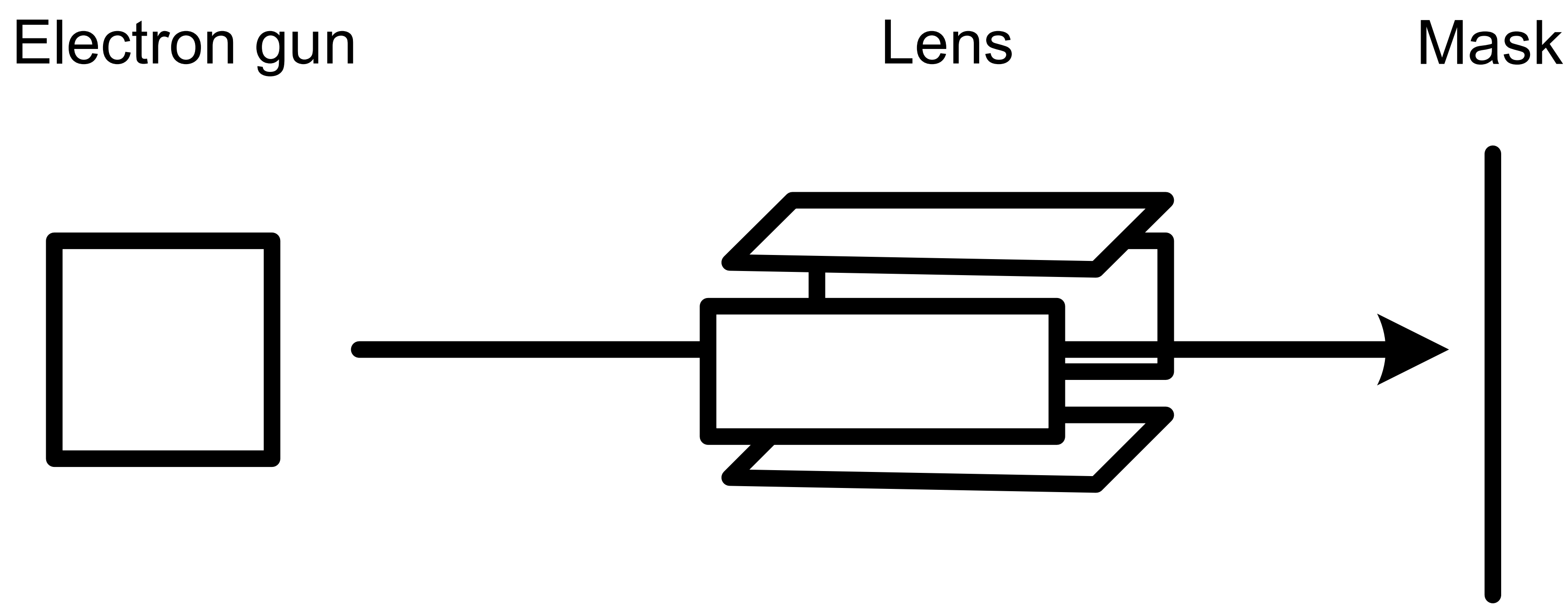
Red = Poly silicon
Yellow = contacts/via
Blue = Metal 1
Yellow = Metal 2
Turqoise = Metal 3
Green = Metal 4

# The complete story



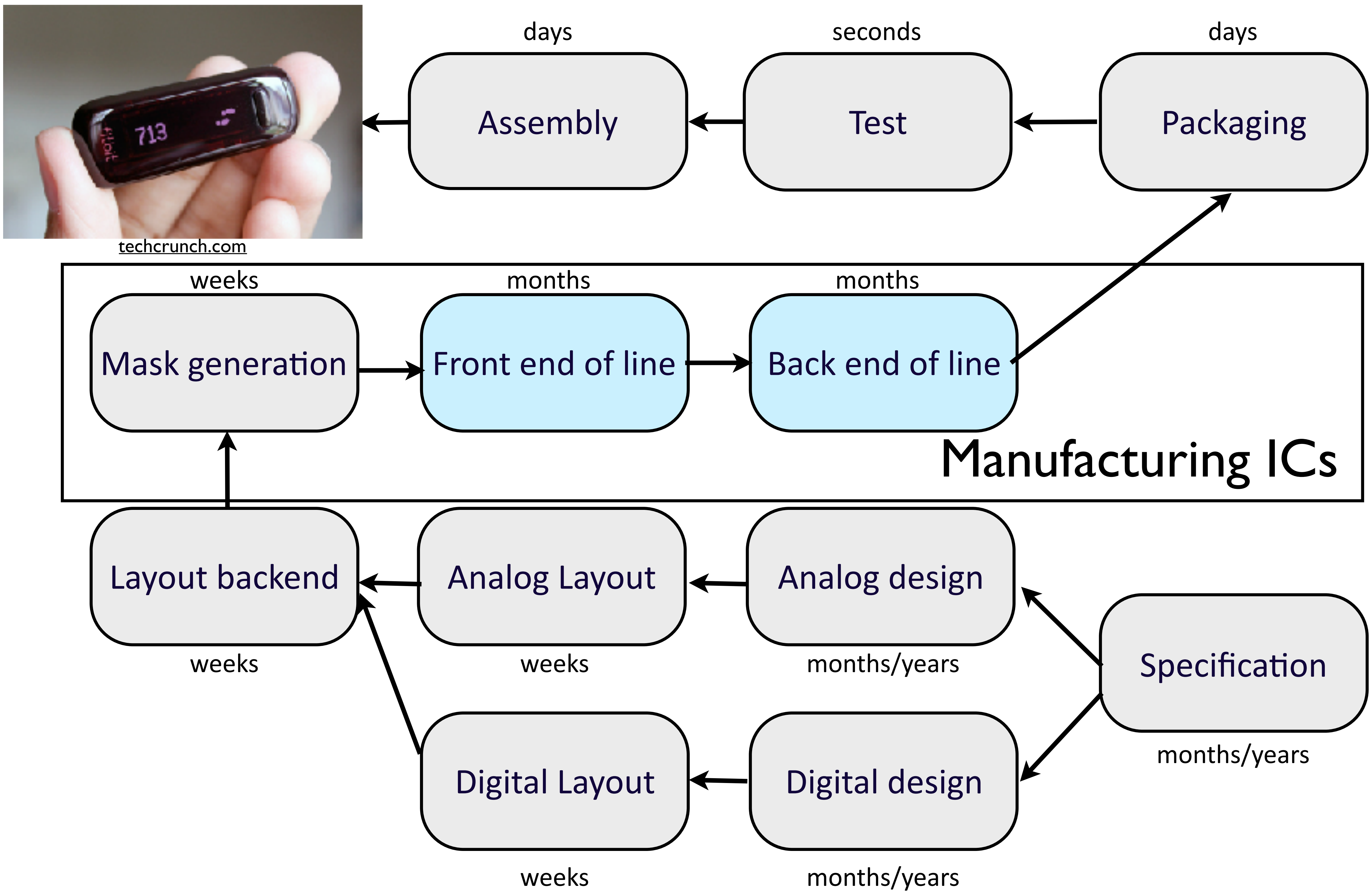
# Manufacturing ICs

# Mask making

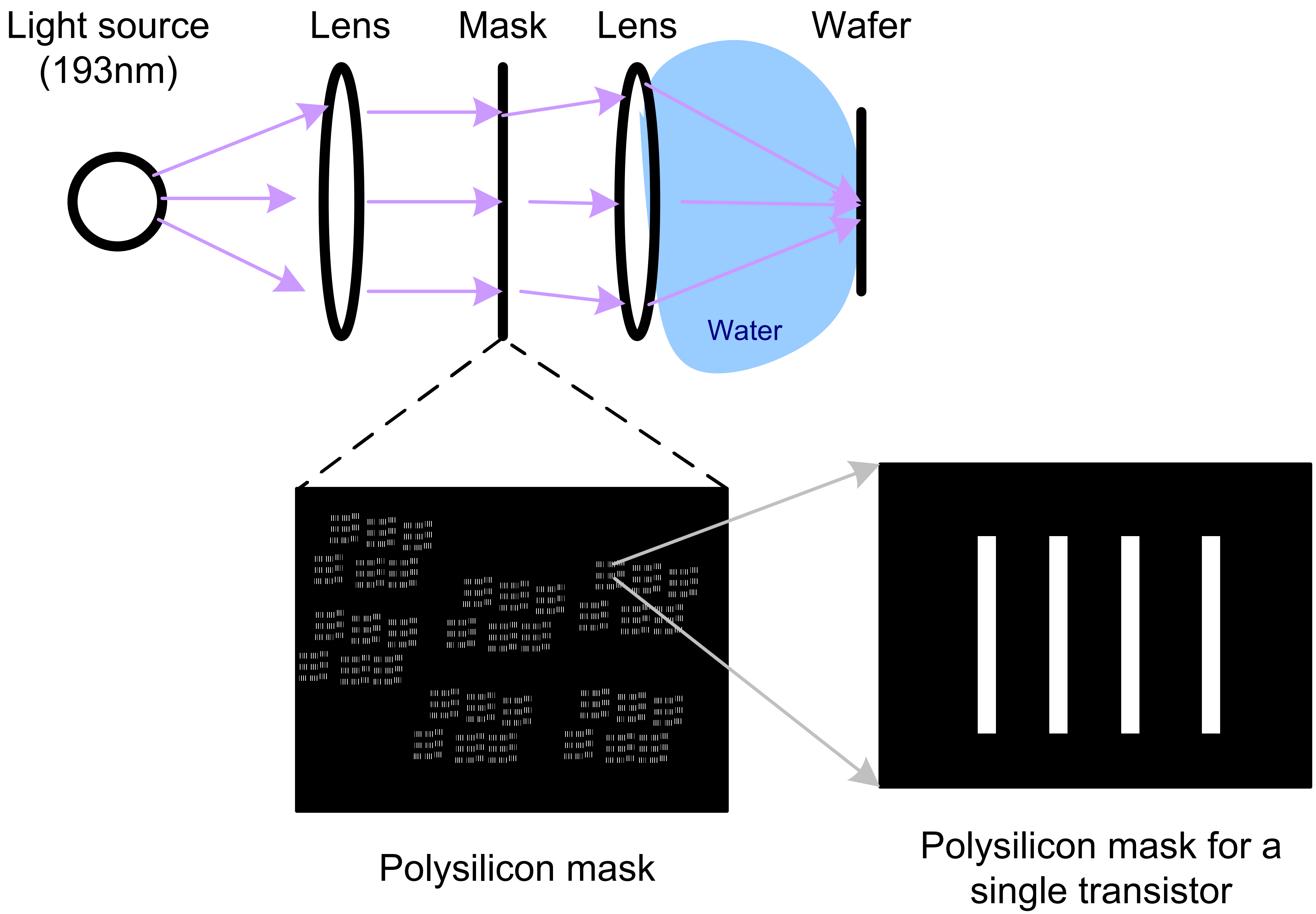



- Mask making is extremely expensive
- A normal chip has around 30 - 40 masks.
- At the 20nm node the mask cost is around 20 million NOK

# The complete story

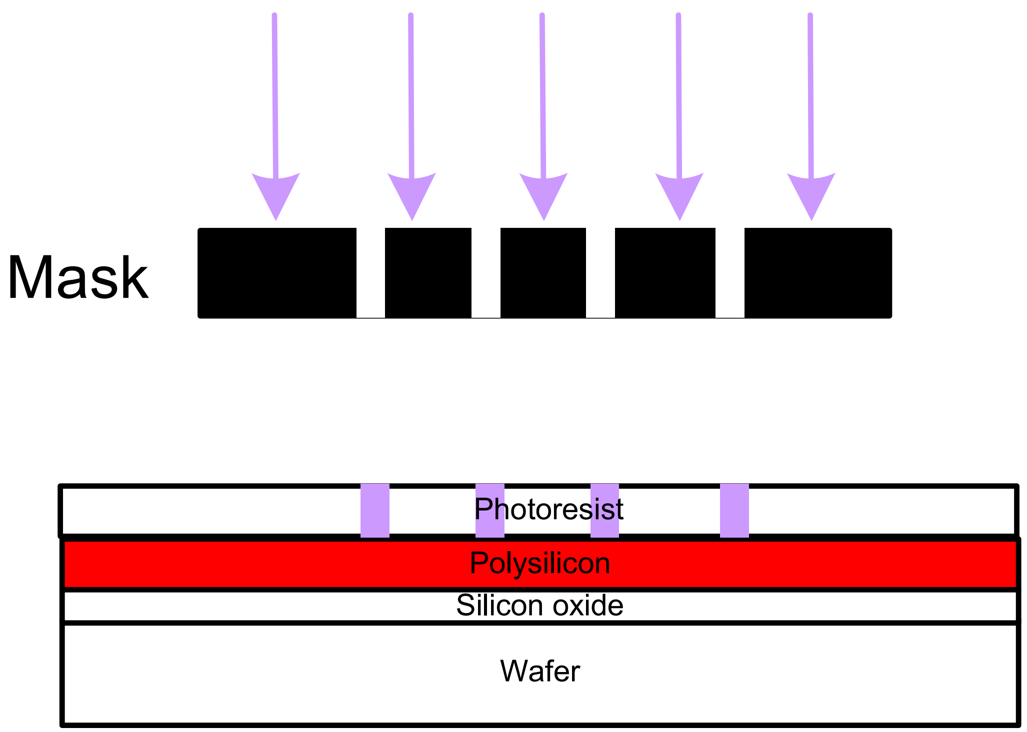


# Lithography

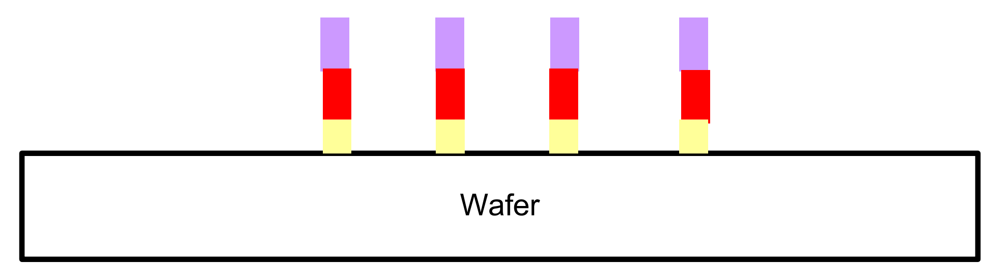



Lithography machines

# Photoresist and lithography

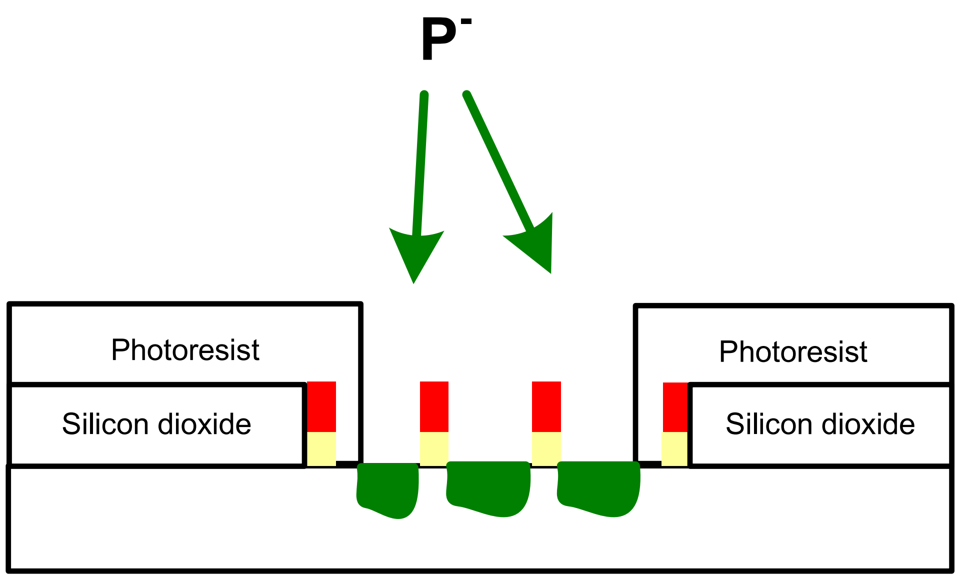



1) Expose photoresist

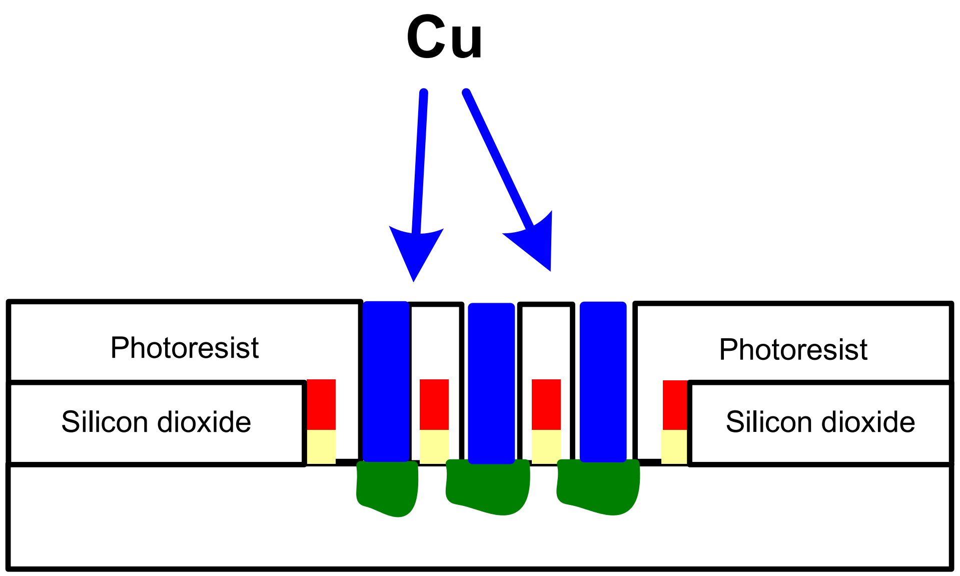



2) Remove photoresist and etch polysilicon

# Doping and metal

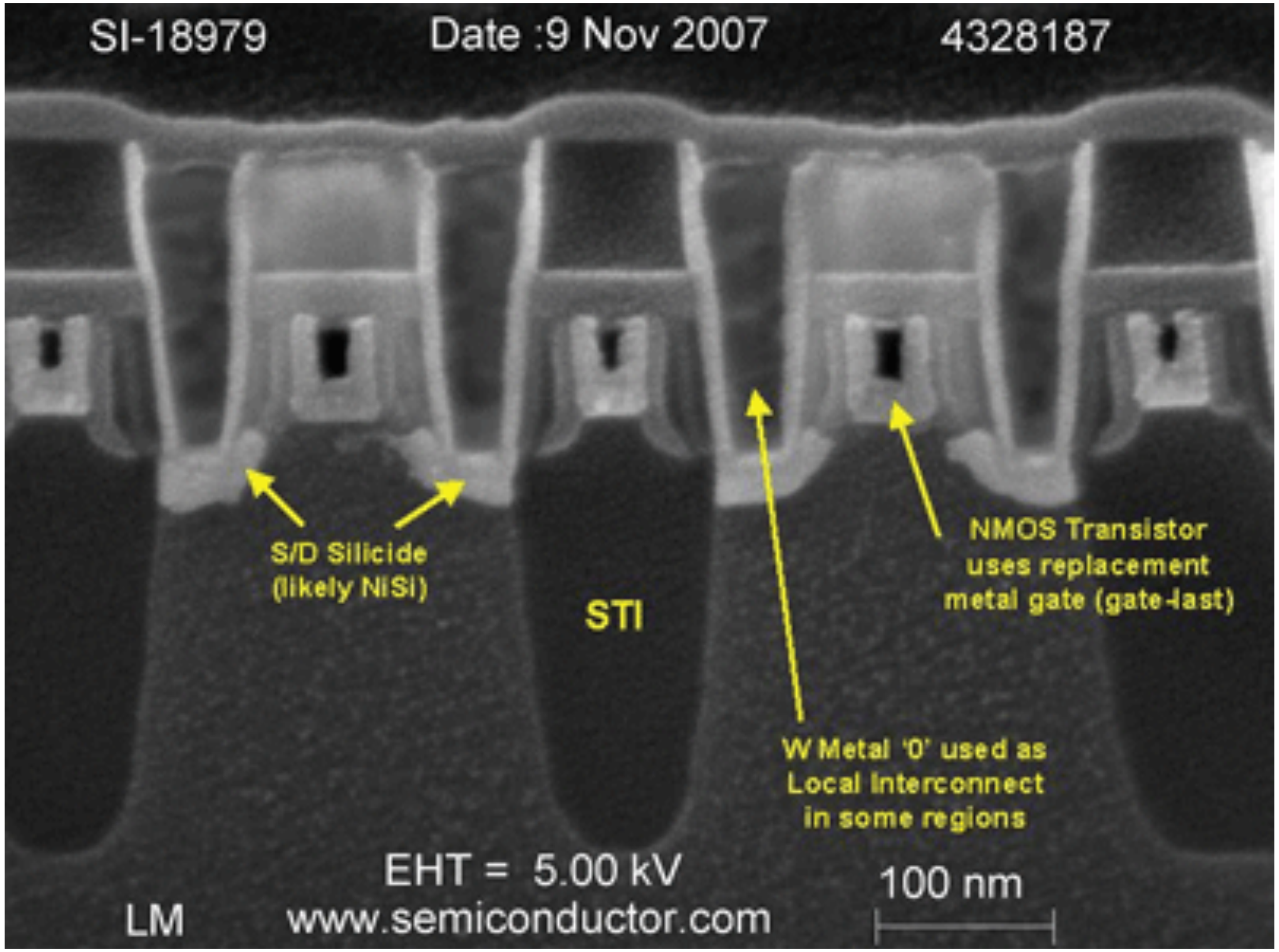



3) Add doping

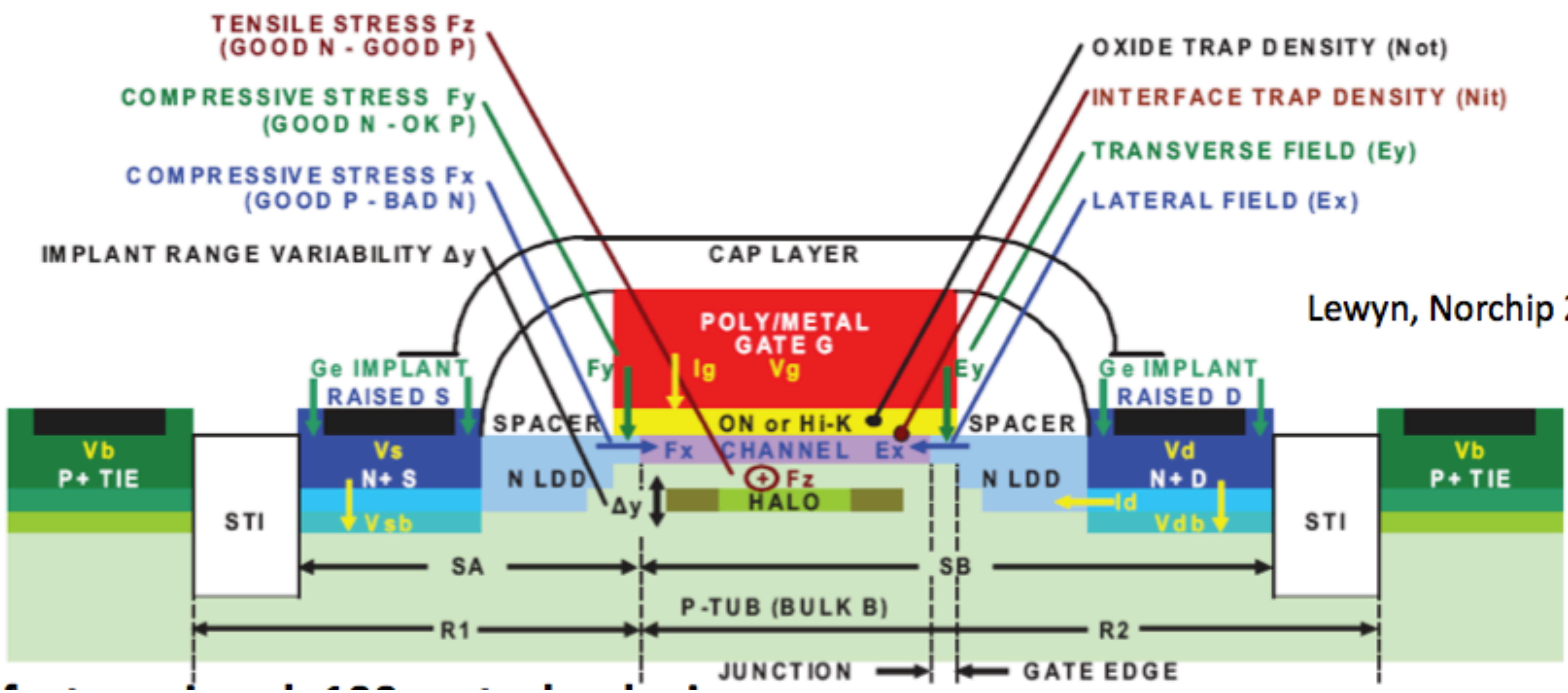



4) Add metal

# Making transistors



# Nano-scale transistor




Lewyn, Norchip 2009

# Today: 193nm argon fluoride excimer laser

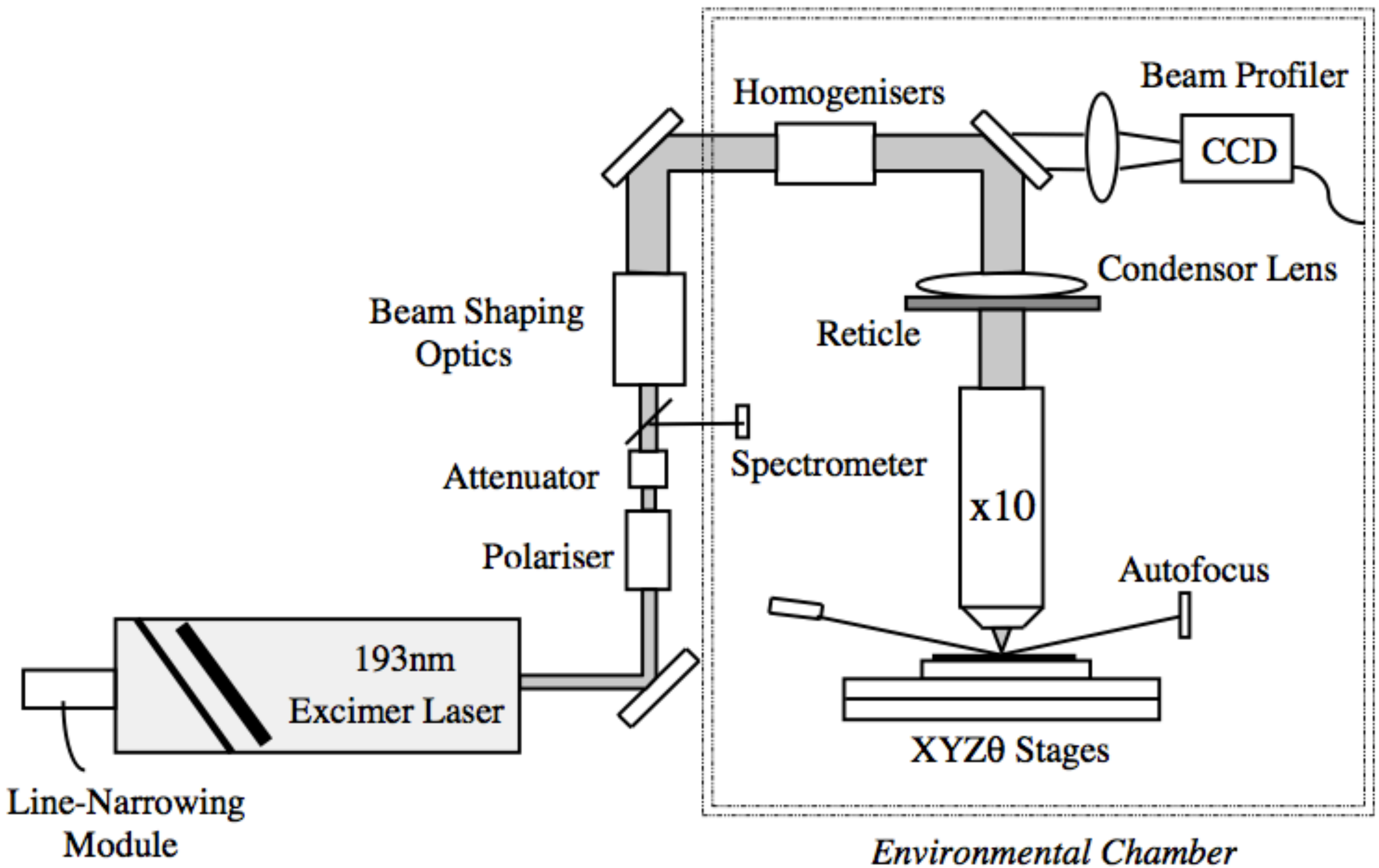
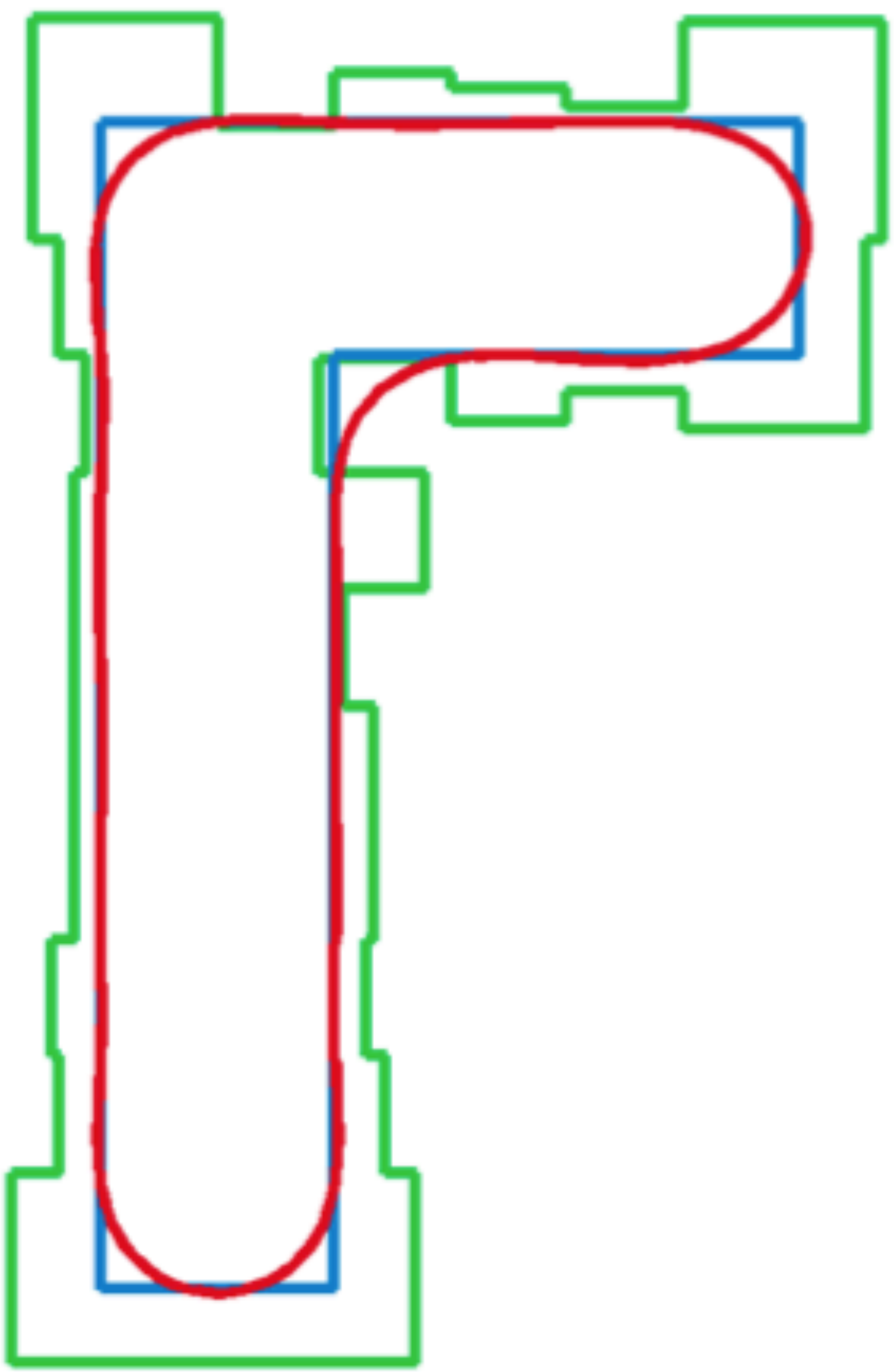



Figure 2. Schematic diagram of 193nm Microstepper

# Optical proximity correction



- The wavelength of the developing light is larger than minimum features ( 193nm > 20nm)
- Diffraction patterns affect the light intensity on the photo-resist
- Extensive calculations need to calculate how the mask should look to compensate for diffraction and processing inaccuracies

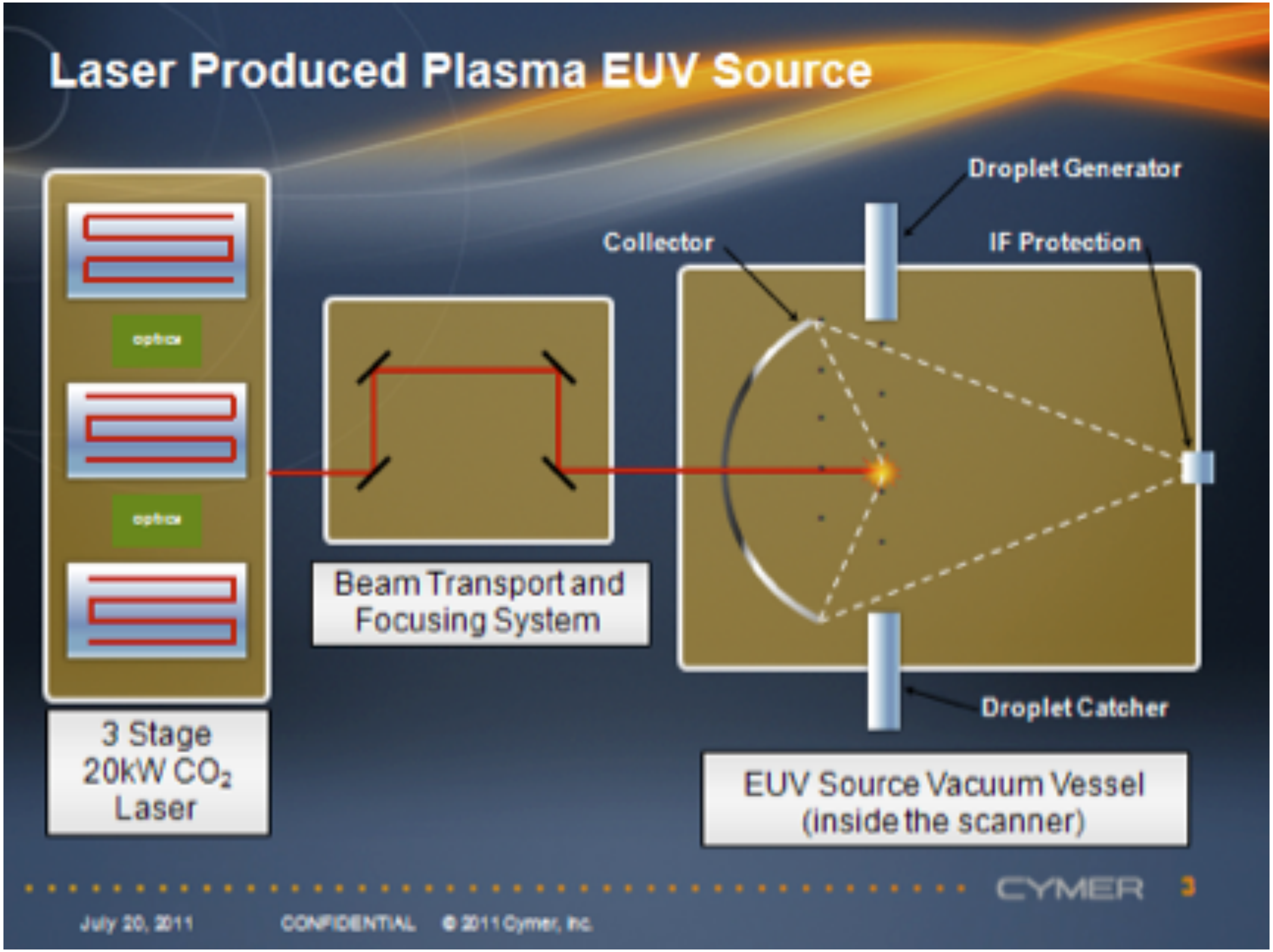
Blue = Pattern we draw in our CAD programs

Green = How the mask actually looks

Red = Pattern on chip

http://upload.wikimedia.org/wikipedia/en/6/65/Optical_proximity_correction.png

# Tomorrow (maybe): Extreme ultra violet




http://www.cymer.com/euv_light_sources/

EUV lithography

# “At least another decade”: What Next?

# Topics not covered

- Simulation, corner verification
- Digital design (Verilog)
- System level design (Matlab)
- Project management
- Lab testing
- Writing documentation
- Writing patents

# What to focus on the next five years

# Divide and conquer

- Break complex stuff into smaller pieces
- Ignore the difficult stuff, and try to get an approximate understanding, then add in the difficult stuff
- Don’t be afraid if something is difficult
- Don’t think you’re stupid and won’t be able to understand
- Don’t think that everybody else is smarter than you

# What you need to teach yourself

- Ability to work hard (constant speed)
- Ability to focus on the important stuff
- Programming
- Report writing
- Explaining things to other people

# Lesson 2

Learn your courses, they are important