# ADC techniques for the nanoscale era

2010-09-28
Carsten Wulff

# Outline

- Who am I, what have I done, and what do I do
- Nanoscale effects to worry about
- Reliability effects
- Nanoscale blocks
- Nanoscale layout

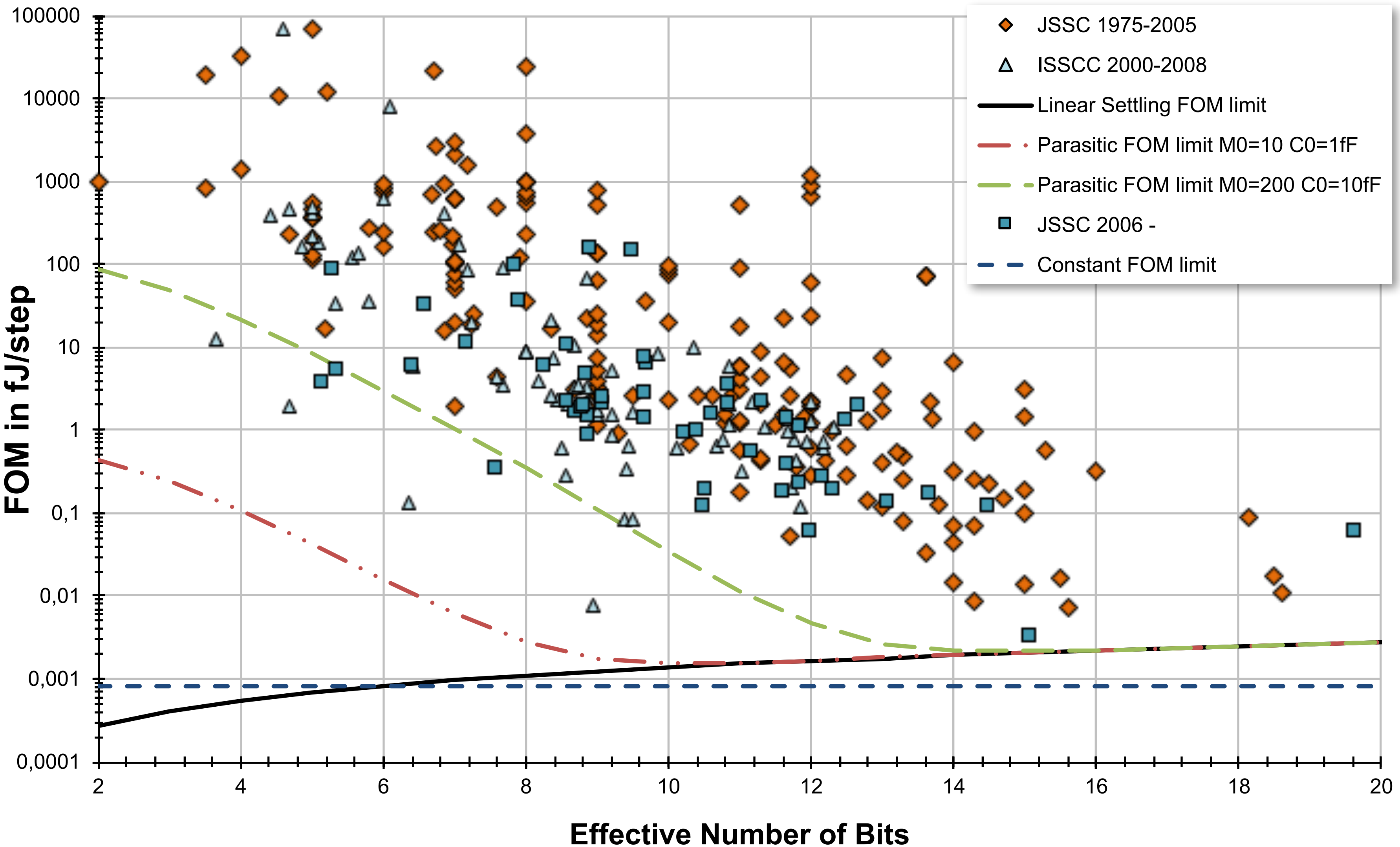
If there is time:

- CBSC and my ADC

# Who am I?

- Carsten Wulff
- Born Friday 13. August 1976
- R & D engineer at wireless department at Nordic Semiconductor
- Married with three kids
- Graduated from NTNU 2002 (Programmable analog integrated circuit with TOC, 0.6um AMS)
- Ph.D from NTNU in 2008 (Efficient ADCs in nano-scale CMOS technology, 90nm ST)
- Fortunate to spend a year at University of Toronto (2006-2007) with David Johns and Ken Martin
- http://www.scribd.com/carstenwulff
- http://www.wulff.no/carsten

# ADC figure of merit




FOM = Power/(2^(2*ENOB)*fs)

# Nanoscale effects

Things to worry about in nanoscale technologies

# Nanoscale papers

CONTRIBUTED PAPER

## Analog Circuit Design in Nanoscale CMOS Technologies

*Classic analog designs are being replaced by digital methods, using nanoscale digital devices, for calibrating circuits, overcoming device mismatches, and reducing bias and temperature dependence.*

By Lanny L. Lewyn, *Life Senior Member IEEE*, Trond Ytterdal, *Senior Member IEEE*, Carsten Wulff, *Member IEEE*, and Kenneth Martin, *Fellow IEEE*

Proceedings of the IEEE, october 2009

## Physical Design and Reliability Issues in Nanoscale Analog CMOS Technologies

Lanny L. Lewyn
LCI, Laguna Beach, California, USA
lanny@pacbell.net

Norchip 2009

# Headroom

- Most nanoscale processes has a power supply of 1-1.2V
- You can run at higher voltages (maybe up to 1.4V), but then you have to worry about hot electron effects
- Consequences:
  - You can't get everything in strong inversion, so just forget about it, use weak inversion when needed.
  - Don't stack transistors too high, so forget about
    - Telescopic OTA
    - Straight cascodes

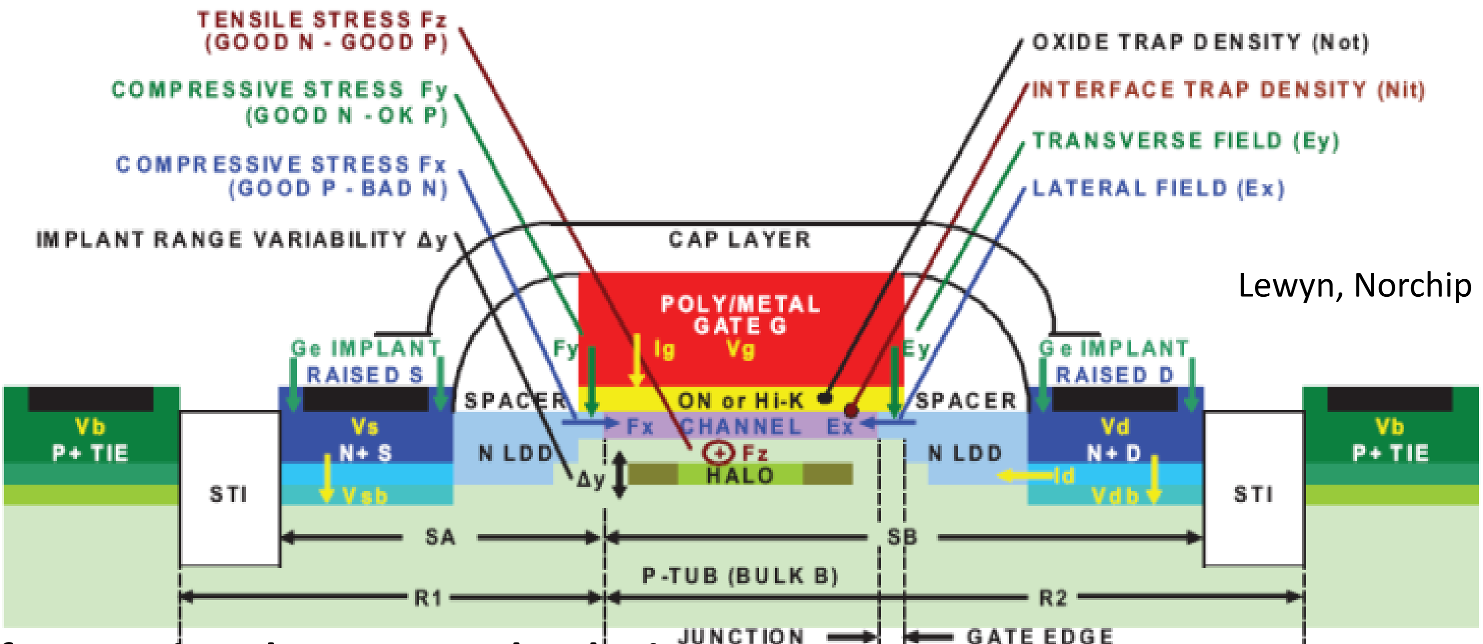
# Headroom, what works

- Wide swing current mirrors (use everywhere)
- Current mirror OTAs or folded cascode OTAs
- Have good control over what is the maximum rating for your process, and run up twoards VMAX (for example in 90nm LP this can be up to 1.45V on VDS)

# Output resistance

- Output resistance of nanoscale transistors is very poor. Don’t expect to get more than 20dB(10x) from a single transistor amplifier
- Use 4F for current mirror transistors
- Use wide swing cascodes everywhere
- Don’t go below 10uA for bias currents unless you really have to

# Nanoscale transistor



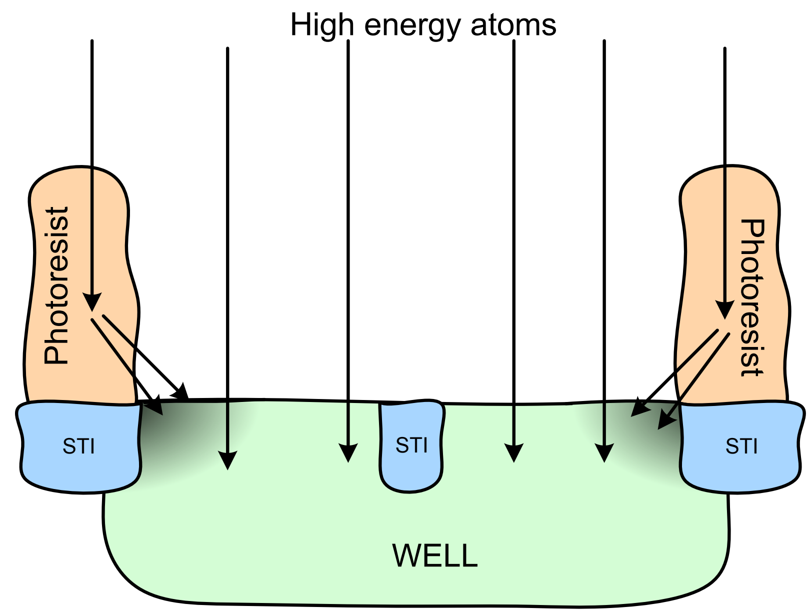

Lewyn, Norchip 2009

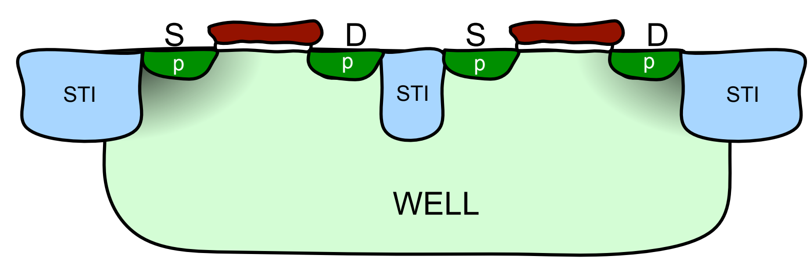
**New features in sub 100nm technologies:**

- Stress is actively used to increase mobility
- Very thin oxide, reduced power supply to keep vertical field in check
- Halo implant that increases drain-source conductance at longer channel lengths
- Hot carrier effects
- Stress from the STI (shallow trench isolation)
- Proximity to well edge
- Lithography issues since the minimum dimensions are less than the wavelength used to expose the photoresist (λ = 193nm)

# Well proximity

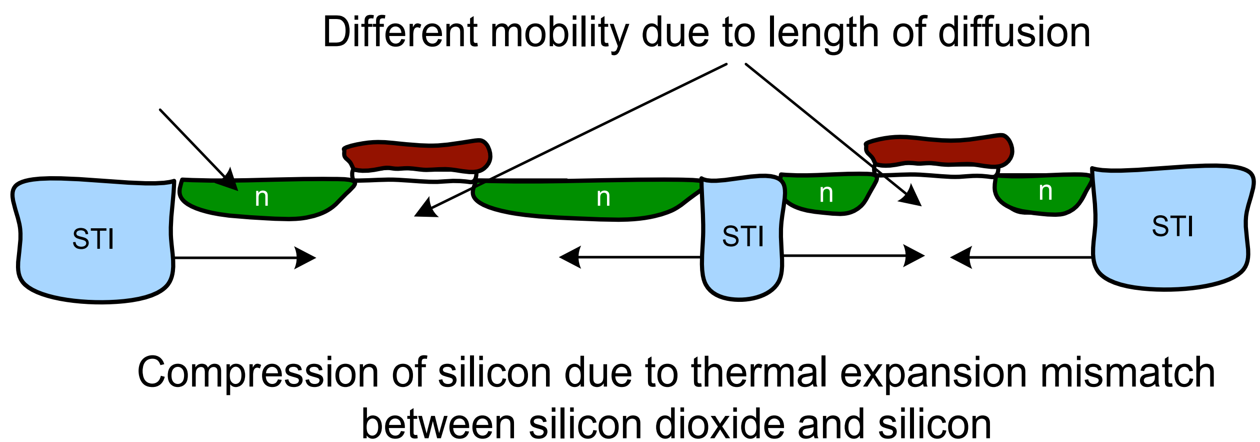
- Threshold voltage increases with proximity to well edge
- Place switch transistors in a transmission gate far from well edge
- Place bias transistors (diode connected transistors) and the transistors they bias far from well edge
- How far is far:
  - Absolute minimum 1.5um
  - Recommended > 2um



# Shallow trench isolation

- Stress is actively used in nanoscale transistors to control threshold voltage




- Use larger than minimum (from DRM) length of diffusion
- Make sure diffusion length set at schematic simulation matches the one used in layout

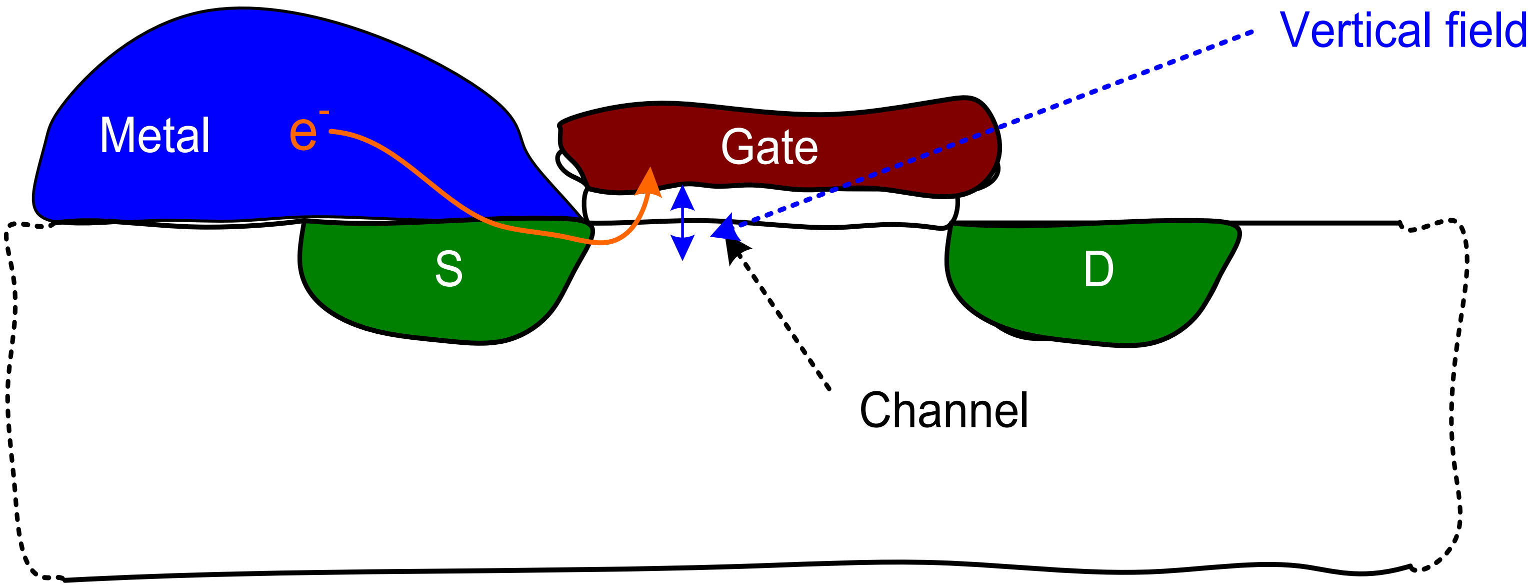
# Reliability effects

TDDB: Time dependent dielectric breakdown - Essential for analog design

HCI: Hot carrier injection - Essential for analog design

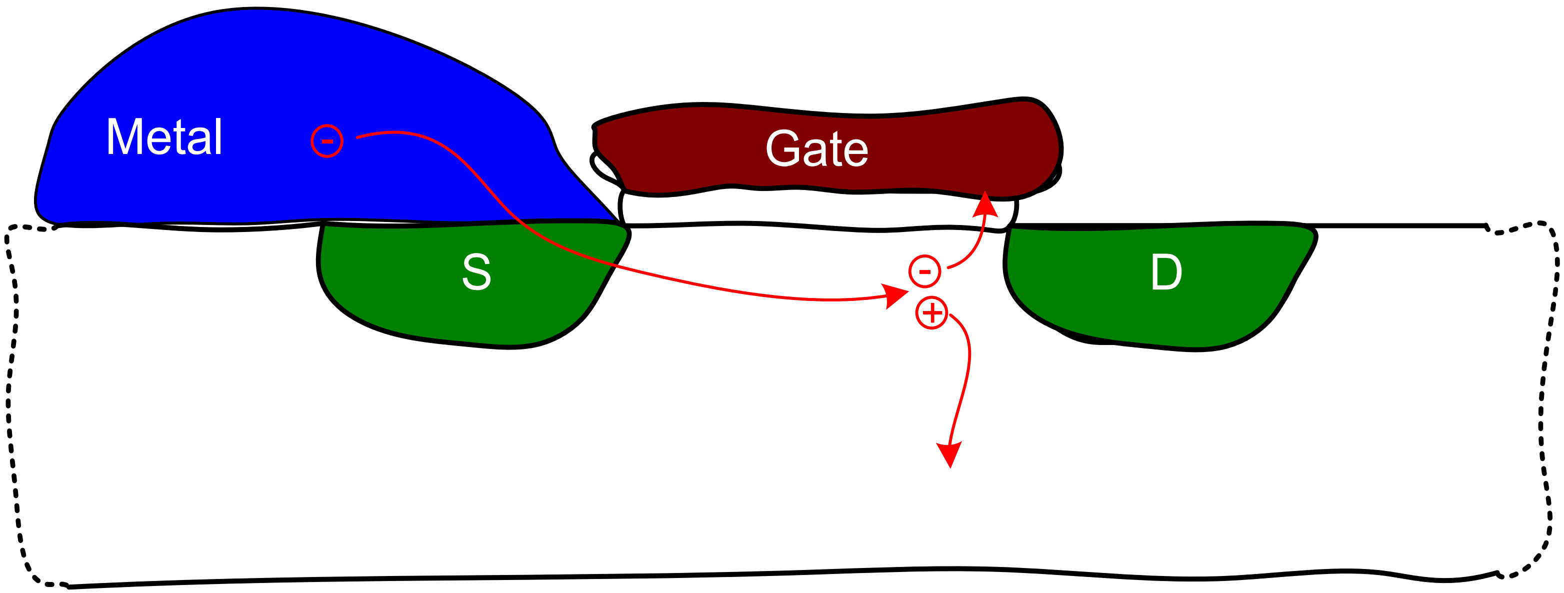
NBTI & PBTI: Negative Bias Temperature instability  - Lanny commented it was not that important for analog design

# Time dependent dielectric breakdown (TDDB)




- \- Electrons (in NMOS) see a high vertical electric field and if this field exceeds around 5MV/cm electrons will go into the gate
- \- Trapped charges in the dioxide shifts the threshold voltage
- \- Can cause a short of the dioxide
- \- This effect sets the maximum VGS

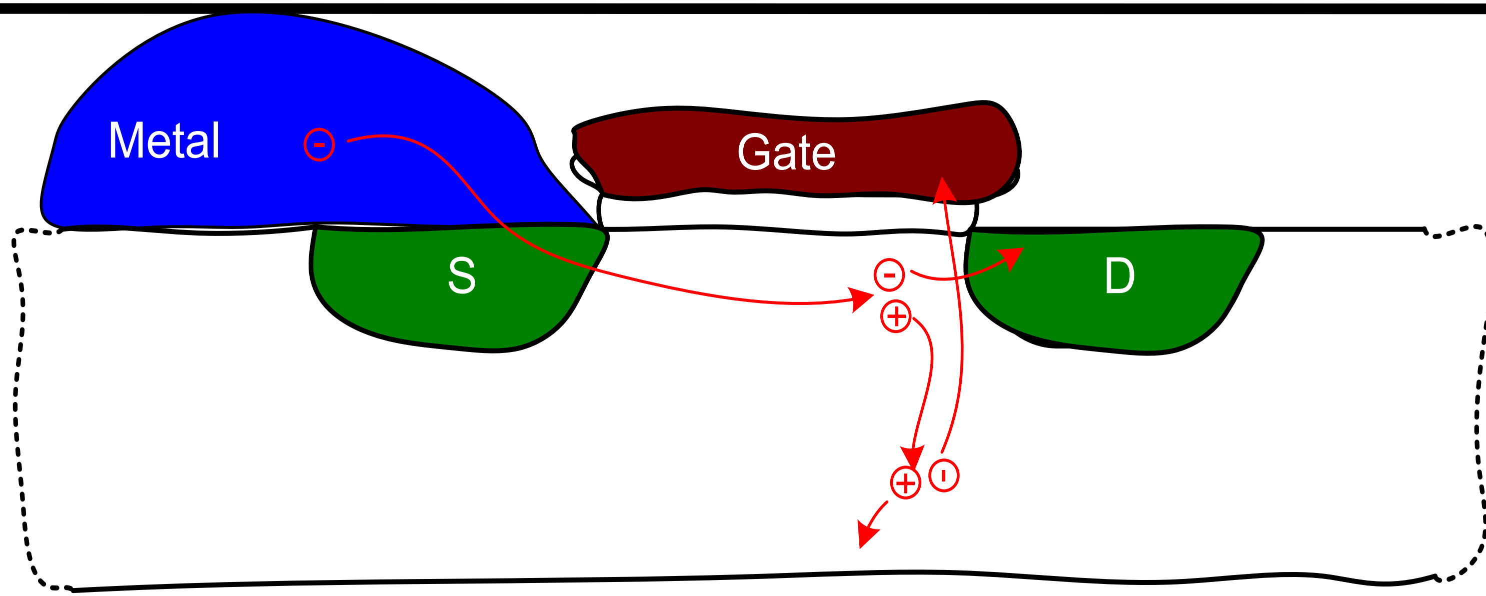
# Hot carrier injection




- - Electron is accelerated due to the high horizontal field (high Vds). It impacts the crystal lattice and generates a electron hole pair.
- - If the impact is high enough energy the electron can pass through the gate and cause damage

**Can occur at moderate $V_{GS}$ and high $V_{DS}$**

# HCI effect: Channel initiated secondary electron




- - An fast electron impacts the lattice and creates a hole-electron pair.
- - Due to a high $V_{SB}$ the hole is accelerated towards the substrate. It can impact the lattice again and make a new hole-electron pair.
- - The secondary electron sees a very high electric field and will accelerate towards the gate

**Sets the maximum $V_{SB}$. $V_{SB}$ ~ $2V_{DD}$ a factor 10 reduced lifetime**

# Nanoscale blocks

F-based design

Typical differential OTA

Typical bias voltage generator

Typical comparator

Differential reference voltage

# F based transistor design

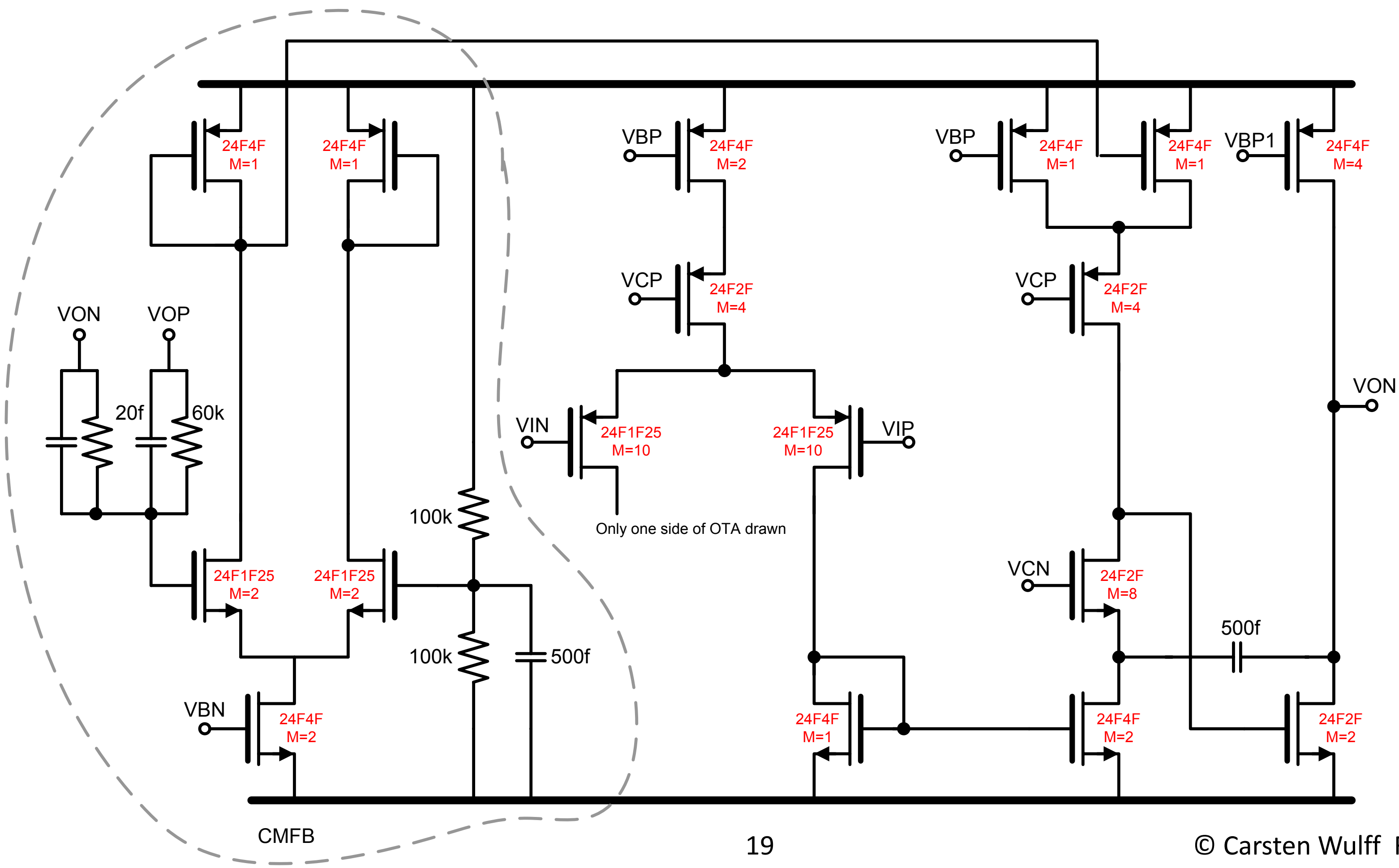
- 1F = 1 gate length
- Why: schematic is independent of technology
- Use a small number of different transistors
- Always use larger than 1F25 length for analog transistors
- Widths: 6F, 8F, 24F

| Lengths | Purpose |
|---|---|
| 1F | Digital transistors, positive feedback inverters |
| 1F25 | Differential pairs |
| 2F | Cascodes |
| 4F | Current mirror transistors |
| 12F | Standalone current mirrors, cascode bias transistors |

# Differential OTA – CM OTA with CT CMFB

Things to watch out for:

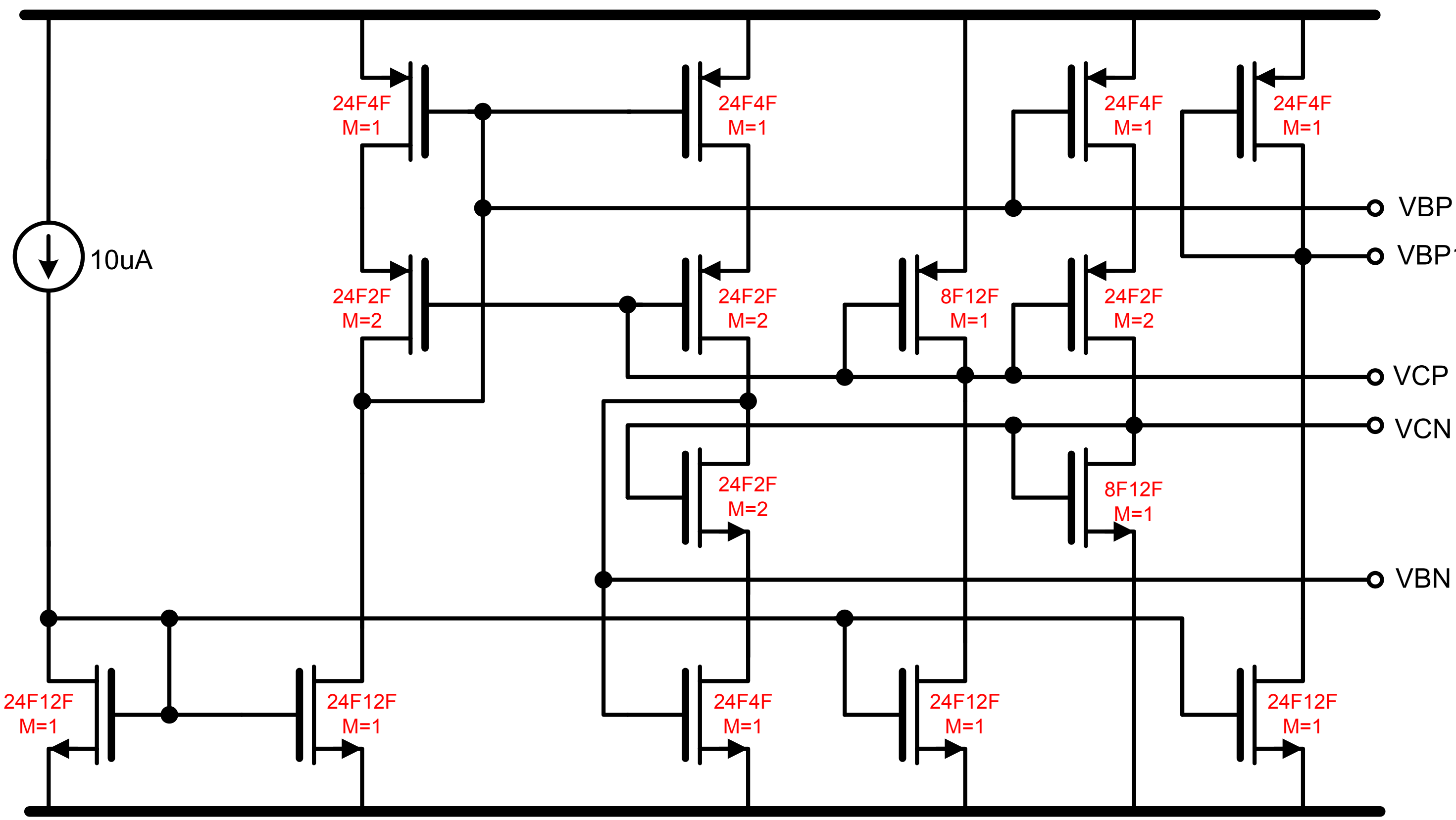
- Common mode stability at high input common modes



# Differential OTA – Bias voltages

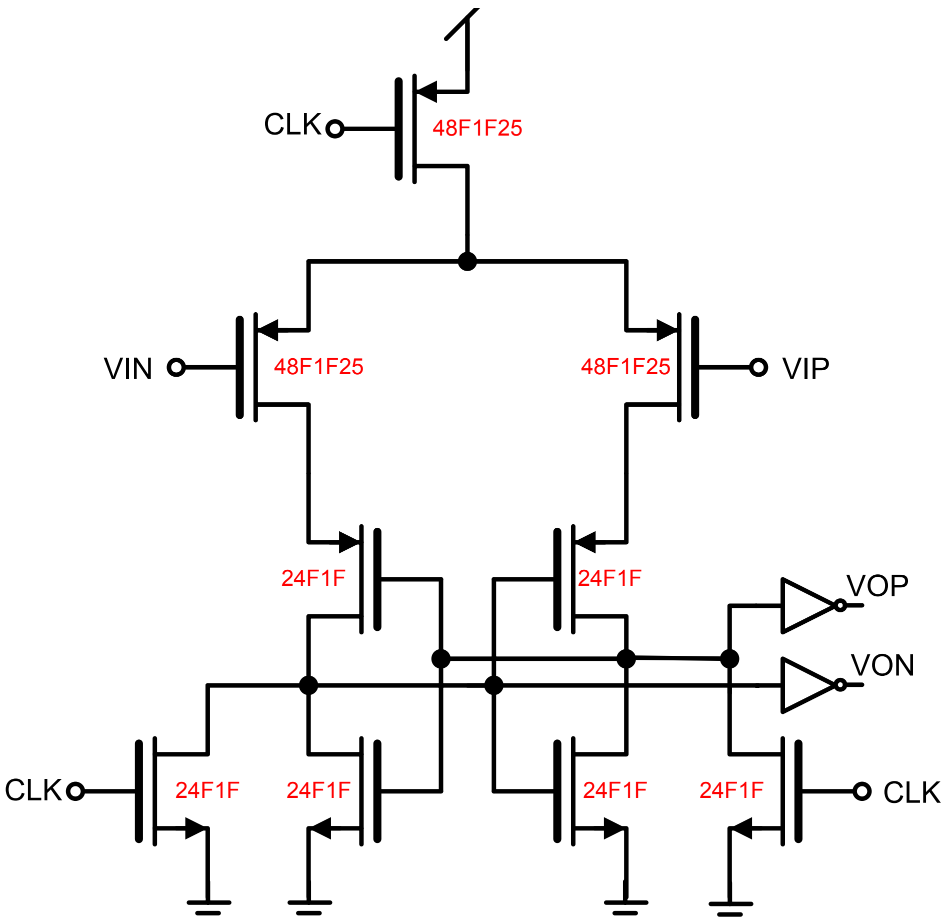
Things to watch out for:

- Current source transistors in saturation over PVT



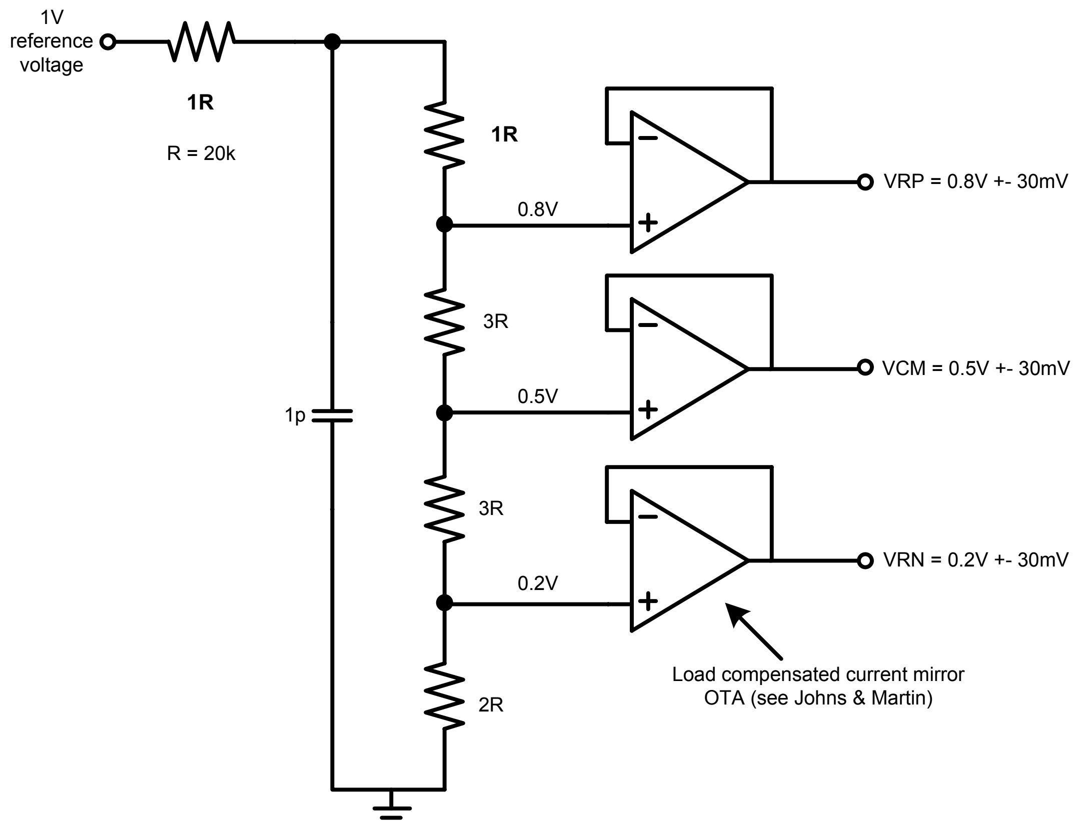
# Differential pair dynamic comparator

- Also called the Strongarm latch
- If mismatch is critical add a preamplifier (differential pair with resistive or diode connected load)



# Differential reference voltage

- If you don't care about gain error, use three unity gain amplifier with a resistive divider at the input. Remember to low-pass filter the input.



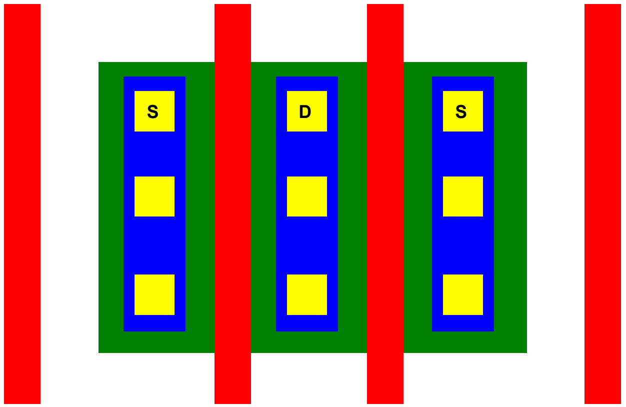
# Nanoscale Layout

Transistor layout rules

Layout example

# Transistor layout rules

| Rule | Why |
|---|---|
| Always use two fingers | Transistor parameters change with current direction |
| Always run all gates in same direction | Stress in X and Y direction affect transistor differently |
| Always have dummy poly | Better poly control during processing |
| Always have larger than minimum length of diffusion | Less stress from shallow trench isolation |
| Always place transistors far from well edge | Reduce mismatch in threshold voltage |
| Be careful with metal routing across transistors | Metal changes the stress in the channel |



# Layout from Lanny Lewyn

- Extremely uniform poly
- Short distance to substrate contact
- All gates in same direction

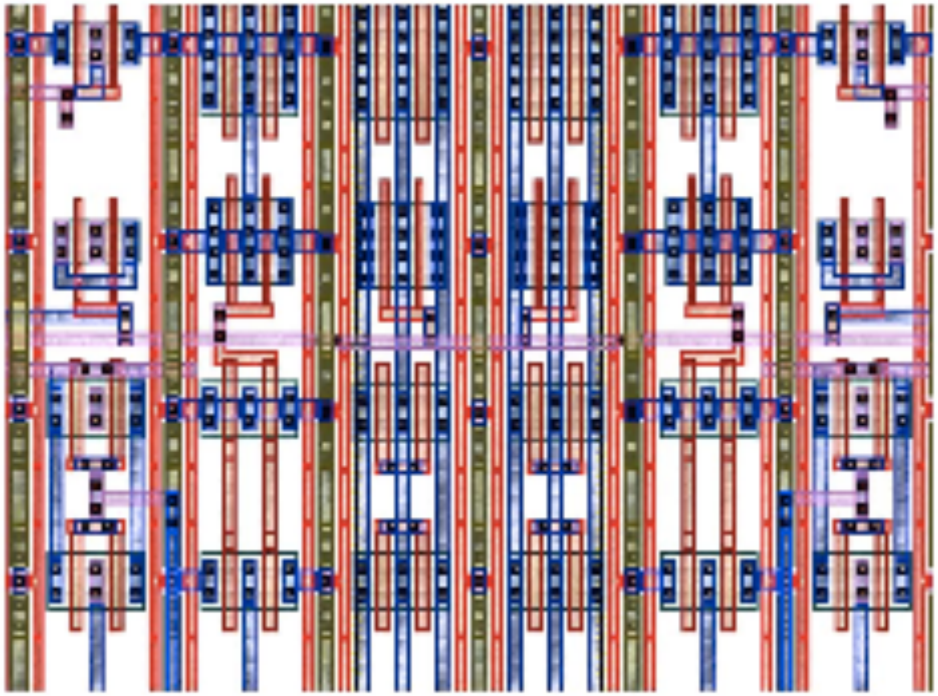


**Fig. 6.** *A portion of an amplifier cell with regular device pitch in both X and Y directions (upper metal layers removed for clarity). For best HF performance, all devices' substrate ties are placed on either side of two-finger gate patterns. Grounded stripes of poly are interposed between device active area and all substrate ties to minimize the need for reticle compensation (OPC) and also reduce poly etch loading to achieve good CD accuracy.*

# Things you should know about

Software:

- Schematic (Mentor graphics, Cadence, Synopsys, Tanner tools)
- Layout (Mentor graphics, Cadence, Synopsys, Tanner tools)
- Simulation (Eldo, Spectre, Hspice, SMASH)
- Scripting (Bash, Perl, TCL, LISP)
- Editors (Emacs)
- Math software (Matlab, Maple, Octave)

Information sources:

- http://ieeexplore.ieee.org
- http://webcast.berkeley.edu/
  - EE240 spring 2007 to spring 2010
- For new tricks, scan JSSC (all papers) each month

# CBSC pipelined ADC with comparator preset, and comparator delay compensation

Carsten Wulff[1], Trond Ytterdal[2]

1. Nordic Semiconductor ASA, Trondheim Norway
2. Norwegian University of Science and Technology, Trondheim, Norway

# Outline

- What are comparator based switched capacitor circuits?
- How was our ADC implemented?
- What was the measured performance of our ADC?

# Sepke et al, ISSCC 2006, 8.5-bit, 8MHz, 2.5mW

**ISSCC 2006 / SESSION 12 / NYQUIST ADCs / 12.4**

**12.4 Comparator-Based Switched-Capacitor Circuits For Scaled CMOS Technologies**

Todd Sepke[1], John K. Fiorenza[1], Charles G. Sodini[1], Peter Holloway[2], Hae-Seung Lee[1]

[1]MIT, Cambridge, MA
[2]National Semiconductor, Salem, NH

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The CBSC concep

+ Completely new approach to switched-capacitor circuits
- Limited speed (dual ramp system)
- Single ended

# What we wanted to do

Primary goals:

- Increase Speed (target 100MHz)
- Differential circuit

Secondary goals:

- Keep resolution (target 8.5-bits)
- High efficiency < 10mW

# What we achieved

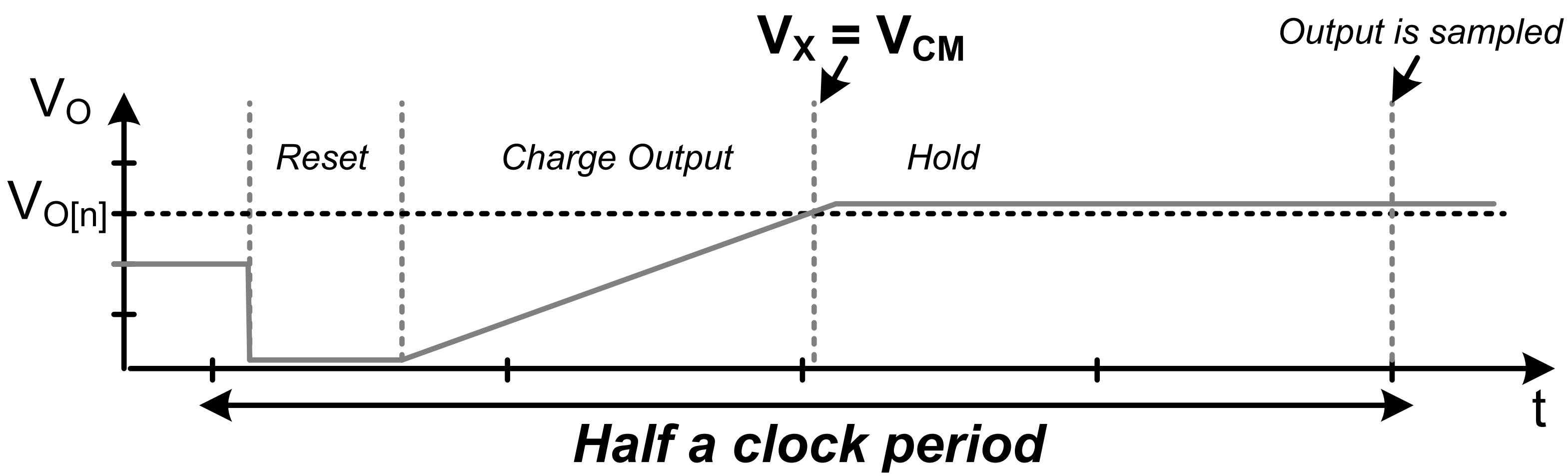
Increased Speed (60MHz)

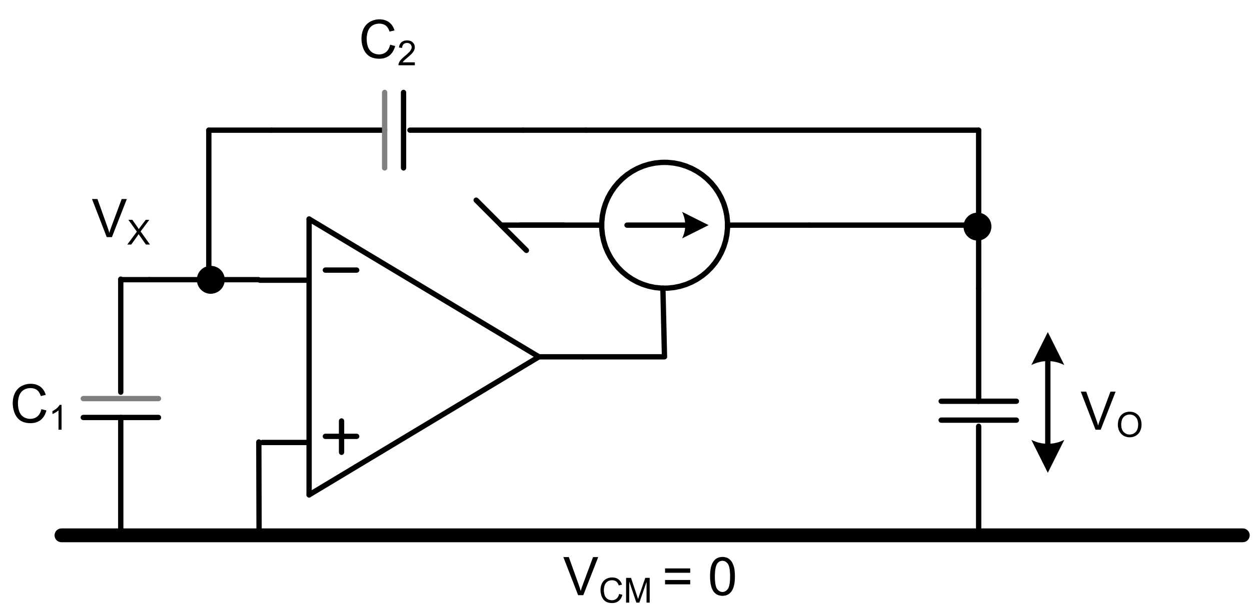
Differential Circuit

Resolution not as high as wanted (7.05-bit)

High efficiency (8.5mW)

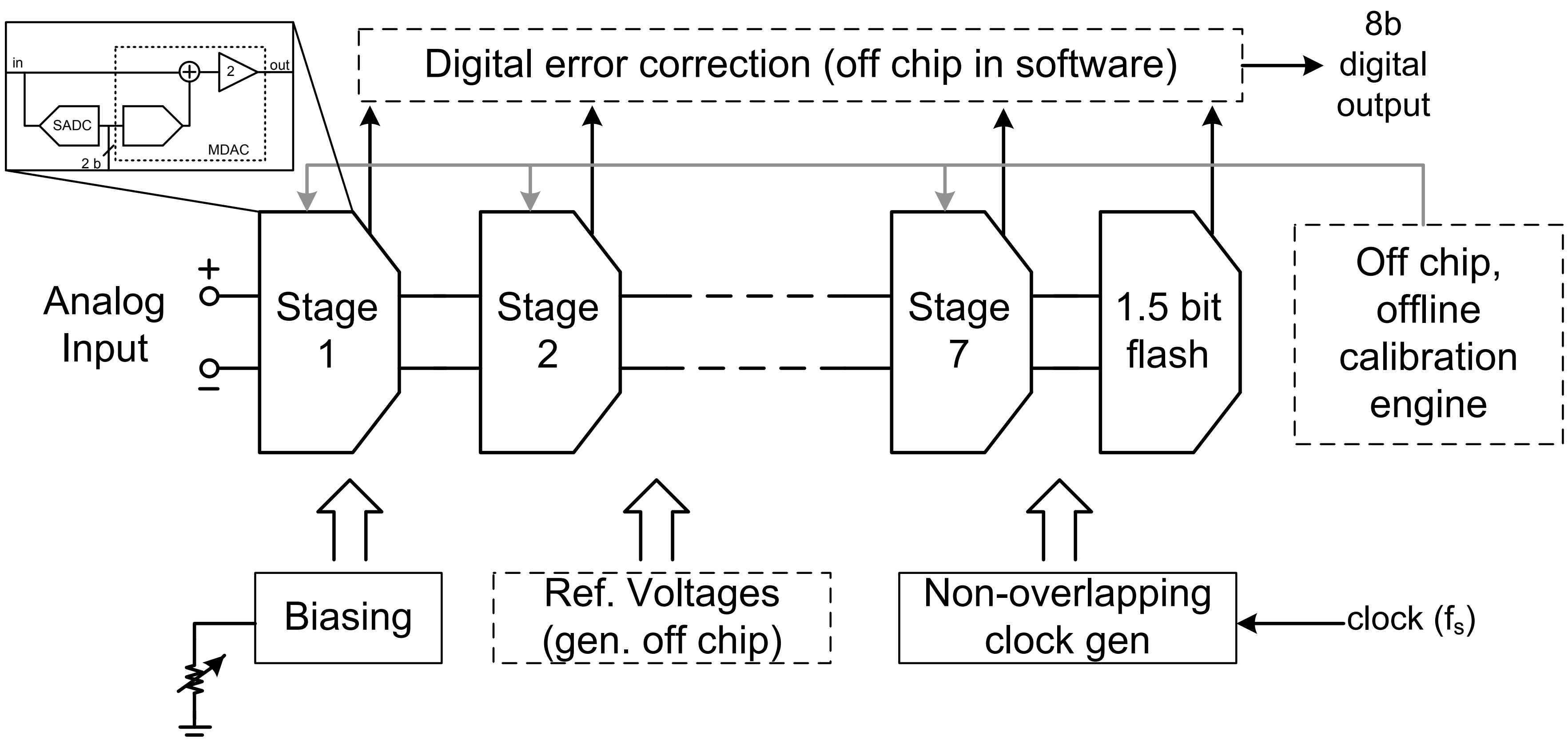
How does a comparator-based switched-capacitor circuit work?



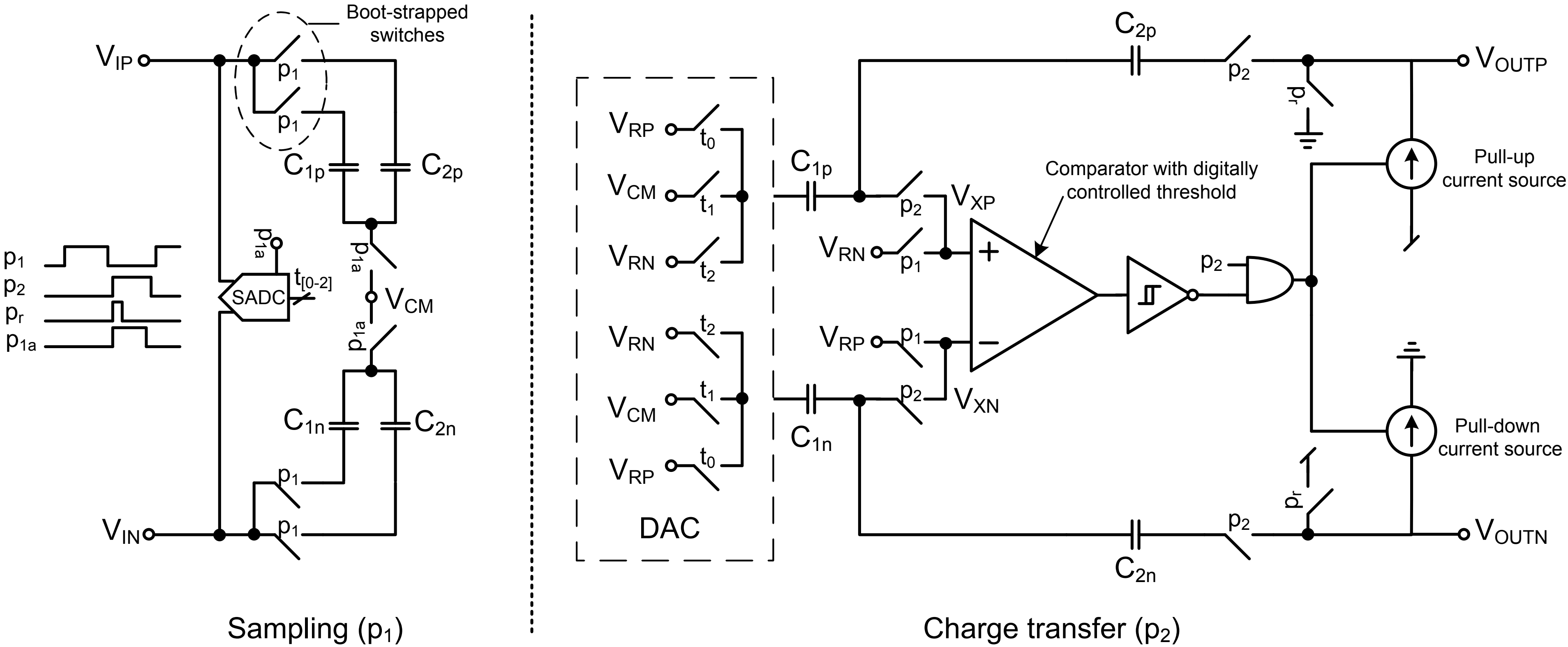



# Implementation

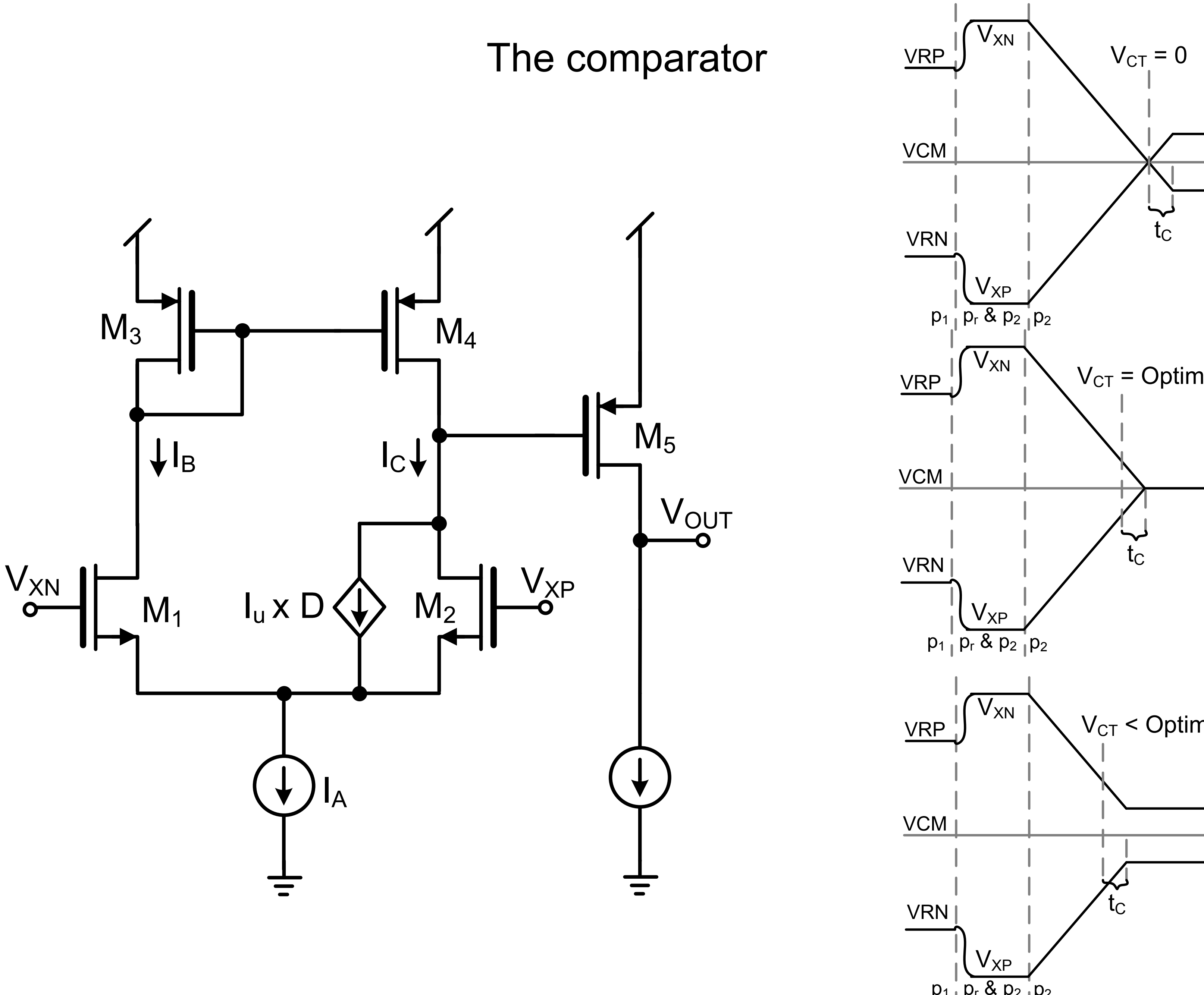
# ADC system block diagram



# The pipelined stage

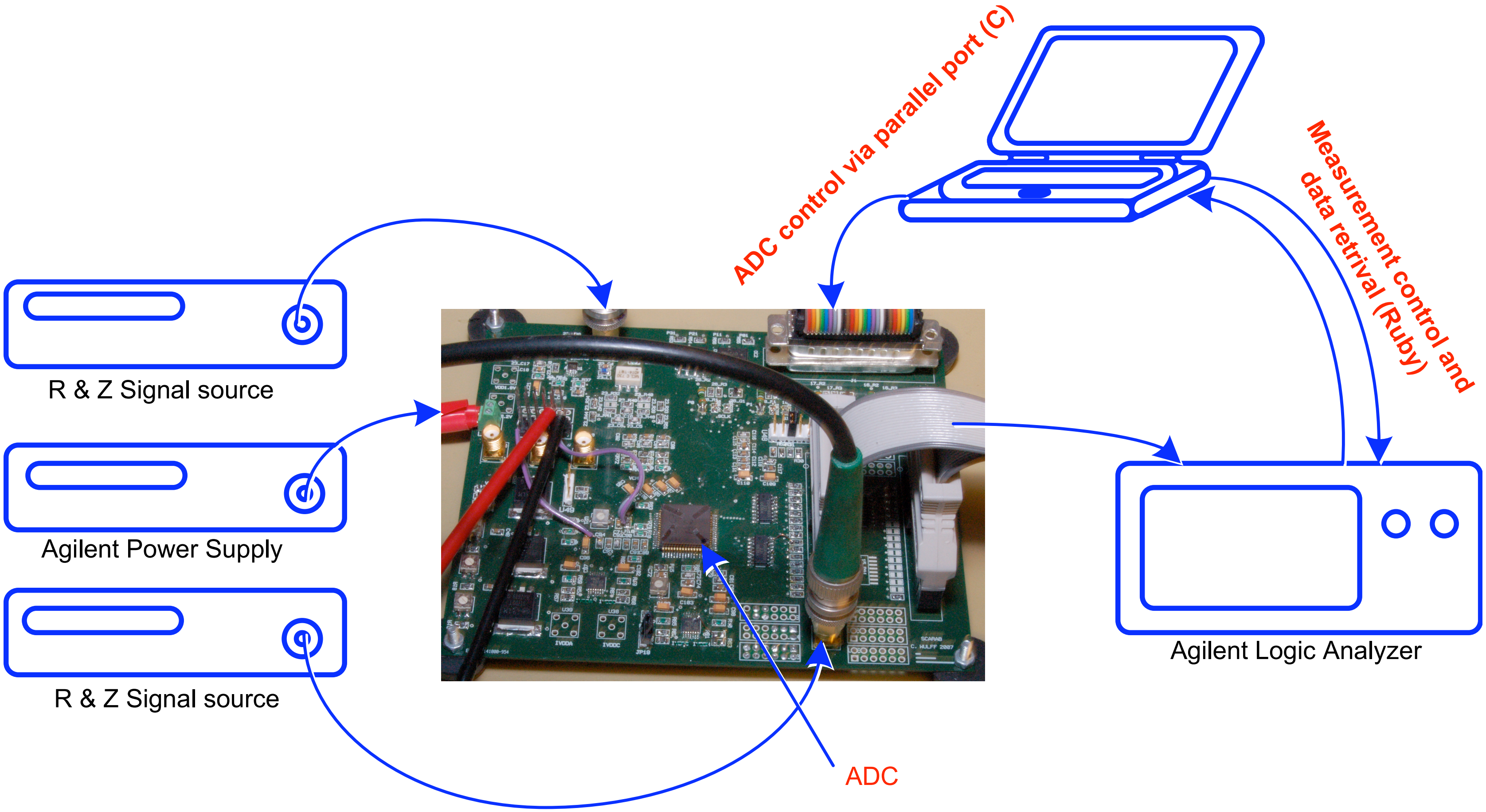


# The comparator



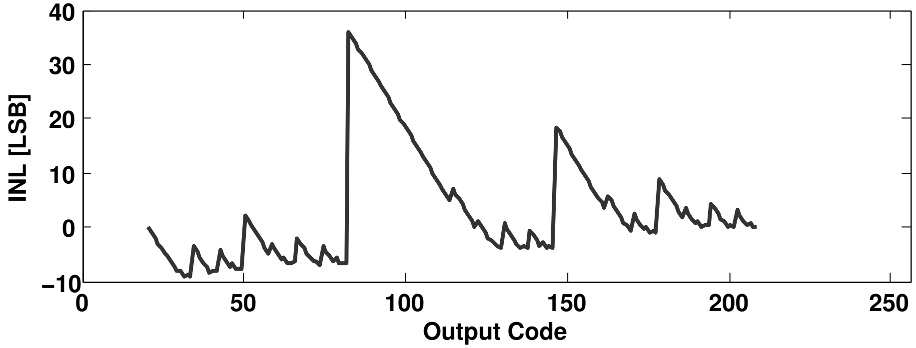
Results

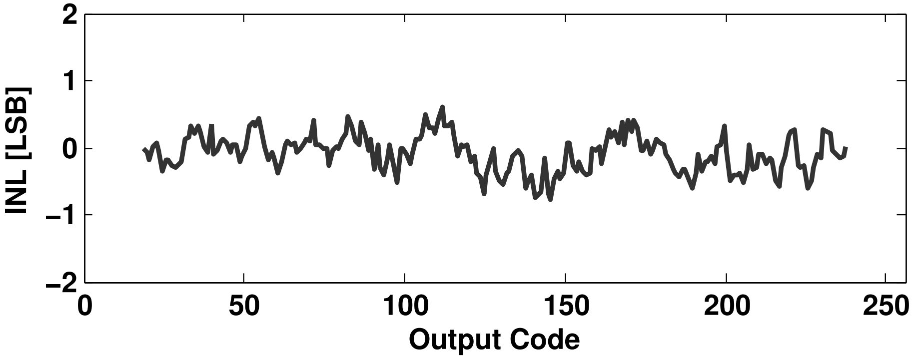
# Lab setup

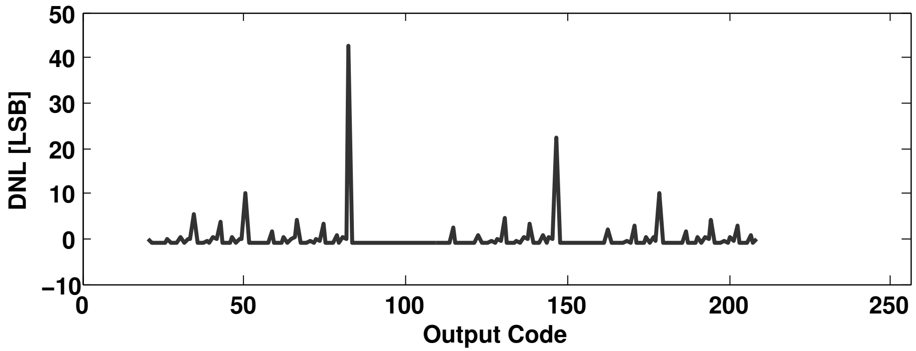

ADC control via parallel port (C)
Measurement control and data retrival (Ruby)
R & Z Signal source
Agilent Power Supply
R & Z Signal source
Agilent Logic Analyzer
ADC

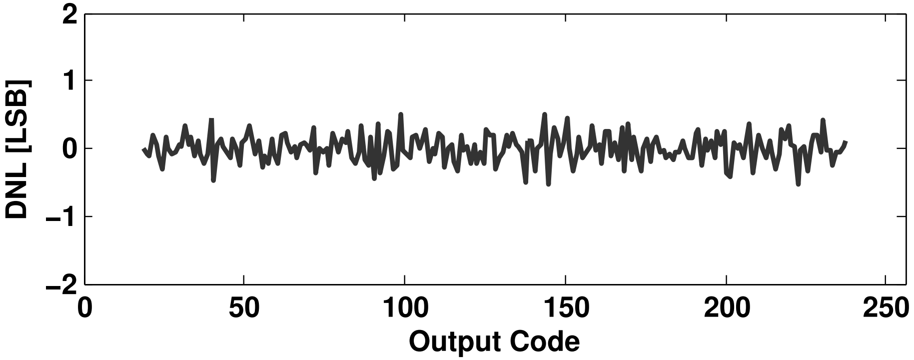
 

# Improvement INL & DNL



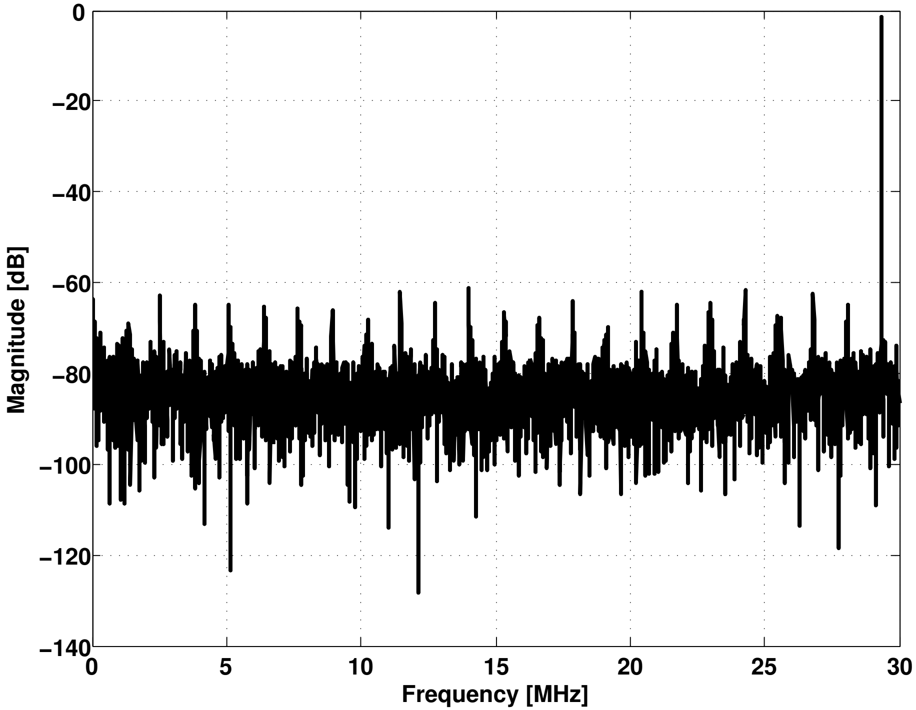

Default values (set before production)

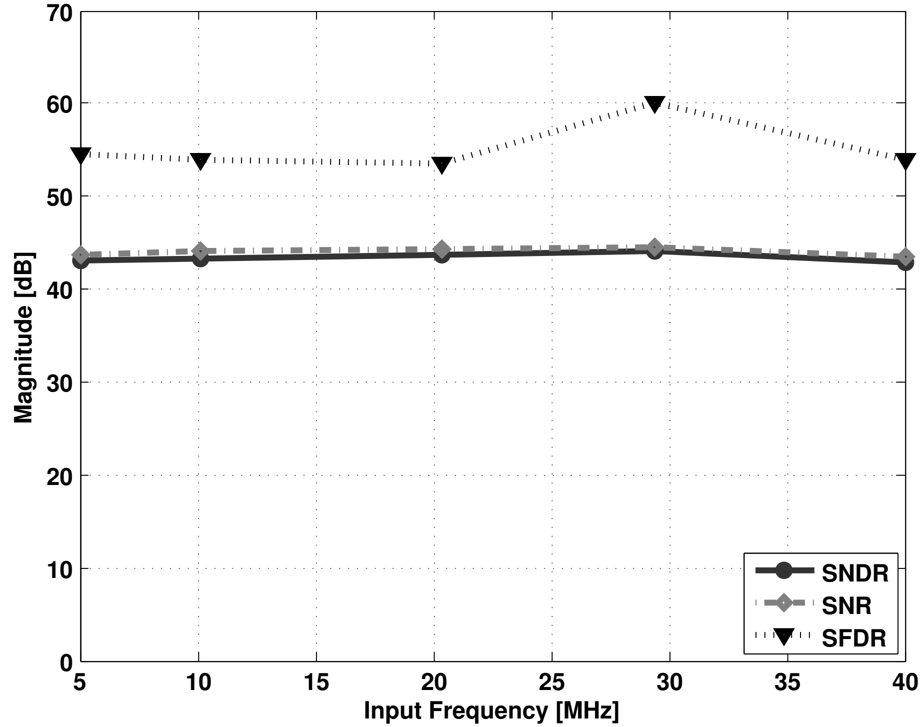
ENOB = 2.5-bit

With calibration

ENOB = 7.05-bit

# FFT, SNR, SNDR & SFDR



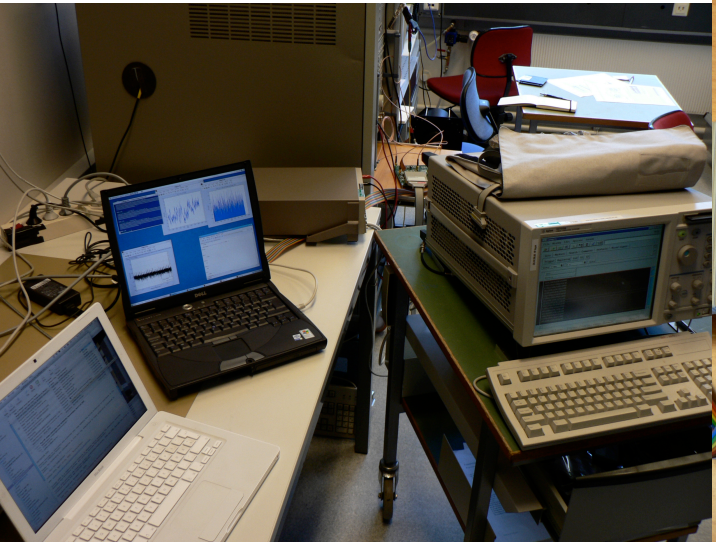
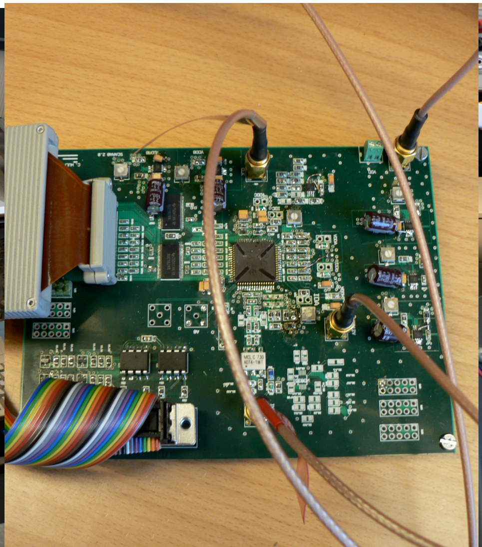

 

# Summary of calibrated ADC performance

| | |
|---|---|
| Technology | 1.2V/1.8V 90nm CMOS |
| Sampling Frequency | 60 MS/s |
| Resolution | 8 bits |
| Full scale input | 0.8V |
| Size | 0.85mm x0.35 mm |
| DNL (LSB) | 0.52 / -0.54 |
| INL (LSB) | 0.6 / -0.77 |
| SNR (29.4MHz input) | 44.5 dB |
| SNDR (29.4MHz input) | 44.2 dB |
| SFDR (29.4MHz input) | 60 dB |
| ADC core power | 5.9mW |
| Clock power | 2.3mW |
| Input switches (1.8V) | 0.3mW |
| Waldon Figure of Merit | 1.07 pJ/step |
| Thermal Figure of Merit | 8.09 fJ/step |

http://www.wulff.no/carsten

Papers, thesis, FOM source data, CBSC modeling, pipelined schematics…


Questions?